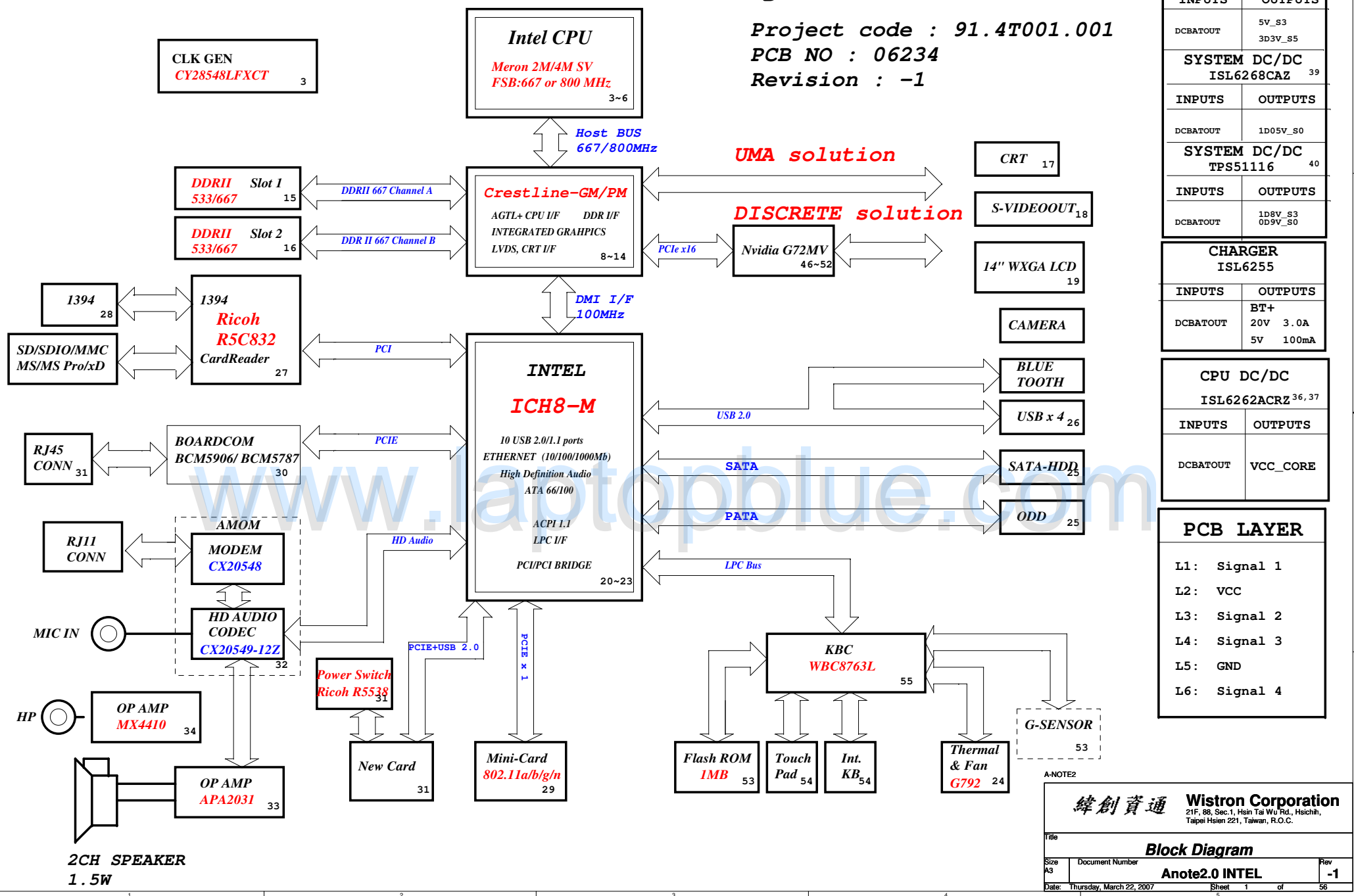


Anote2.0 Block Diagram



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Title
Block Diagram
Size A3 Document Number
Anote2.0 INTEL Rev
-1
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INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCLI_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCLI_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCLI_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCLI_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVP#3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIe port config bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCLI_5		
SM_INTVRMEN	High=Enable	Low=Disable
0	1	High=Enable
1	0	Low=Disable

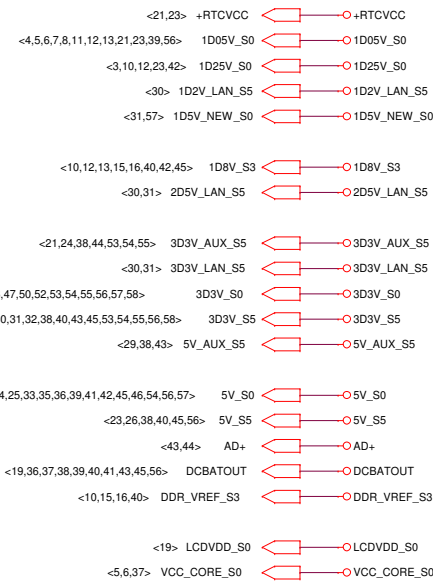
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
0	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD



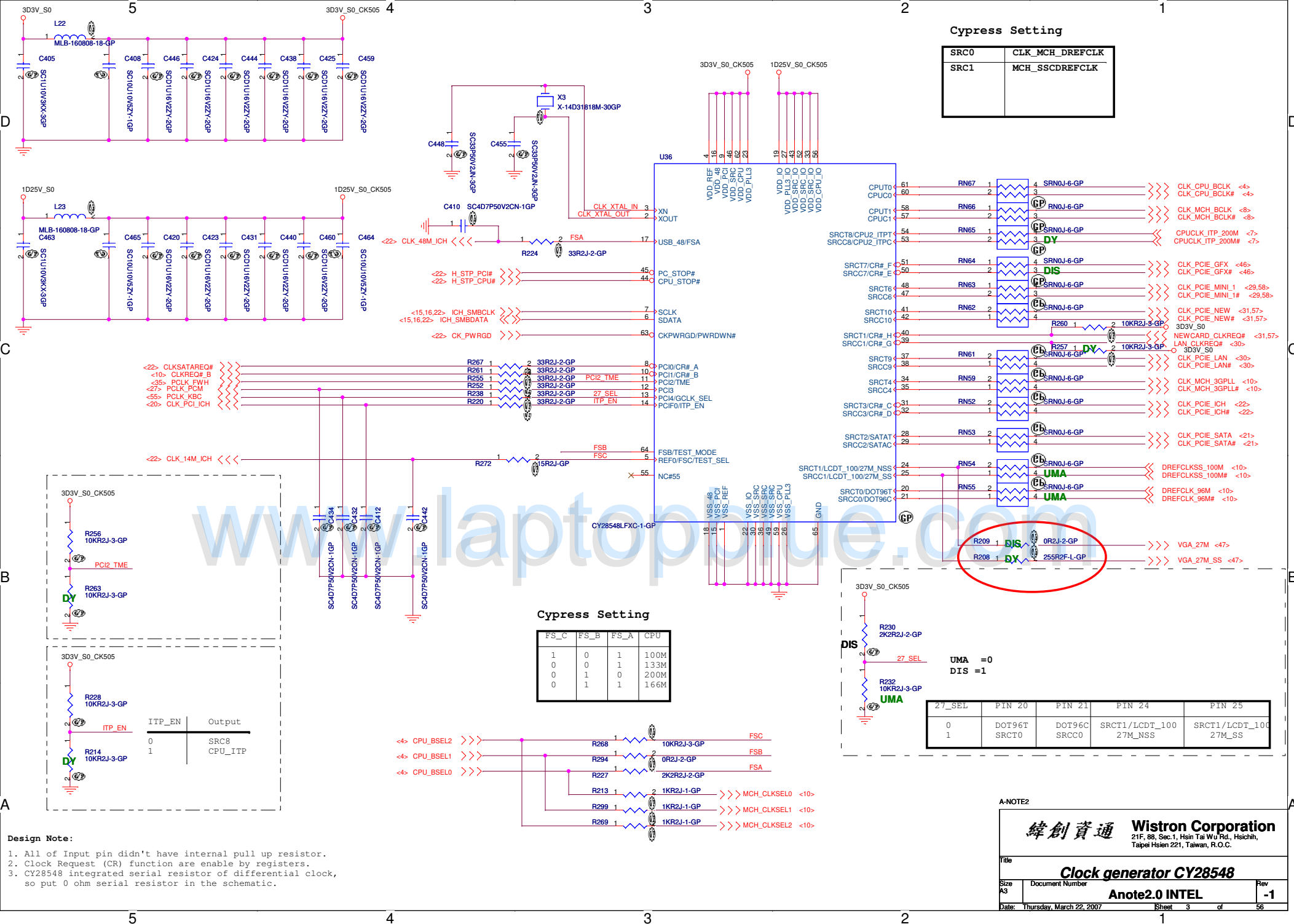
INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8	Low Power PCI Express	Normal ★
CFG 9	PCI Express Graphics Lane Reversal	Normal Mode (Lanes number in order) ★
CFG 16	FSB Dynamic ODT	Disabled
CFG 19	DMI Lane Reserved	Reserved Lane ★
CFG 20	Concurrent SDVO/PCIe	Only PCIe or SDVO is operation ★
SDVO_CTRL_DATA	NO SDVO Card Present ★	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13	Reserved	
LH(00)	XOR Mode Enabled	
LH(01)	All Z Mode Enabled	
HL(10)	Normal Operation	
HL(11)	Normal Operation	

A-NOTE2

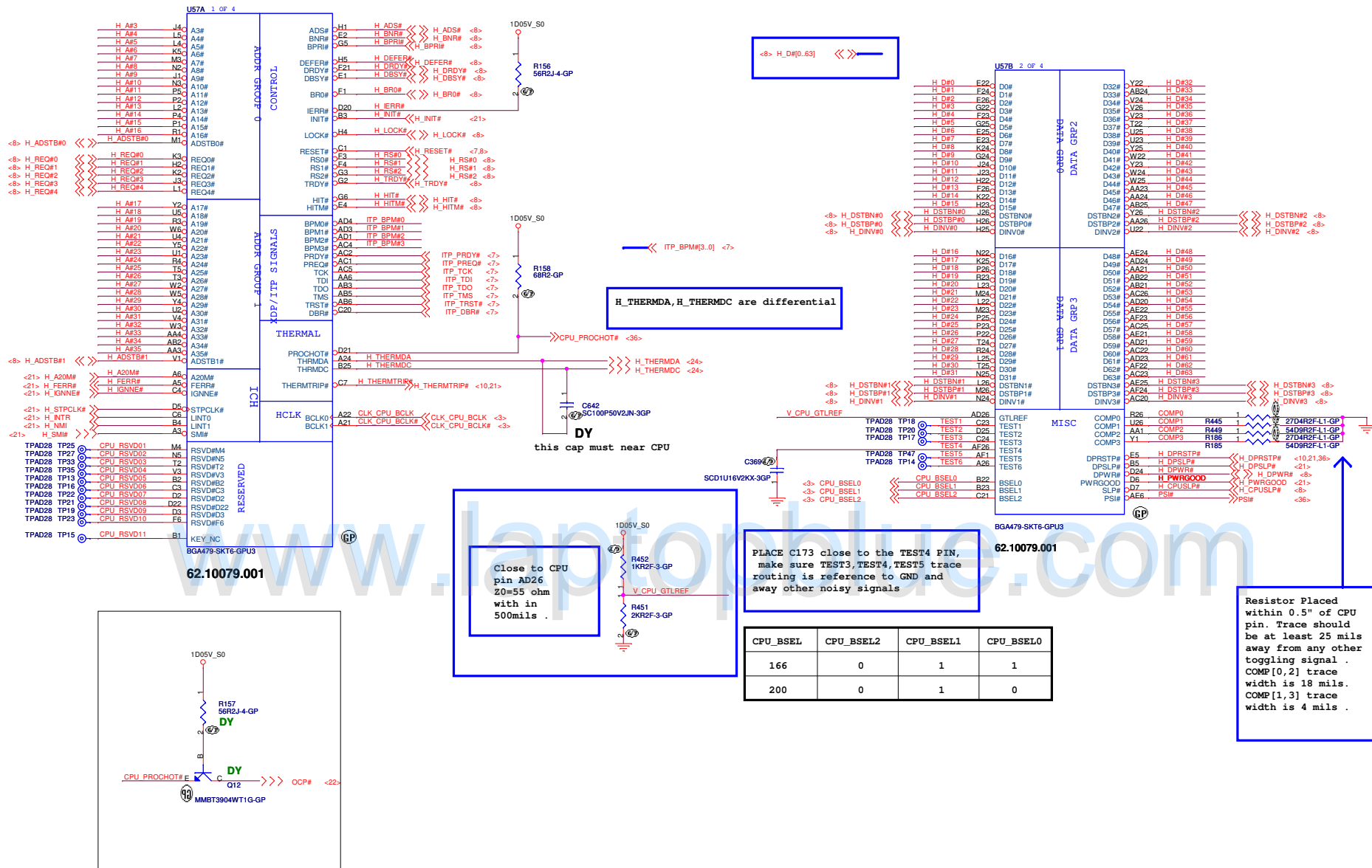
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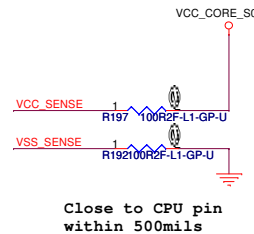
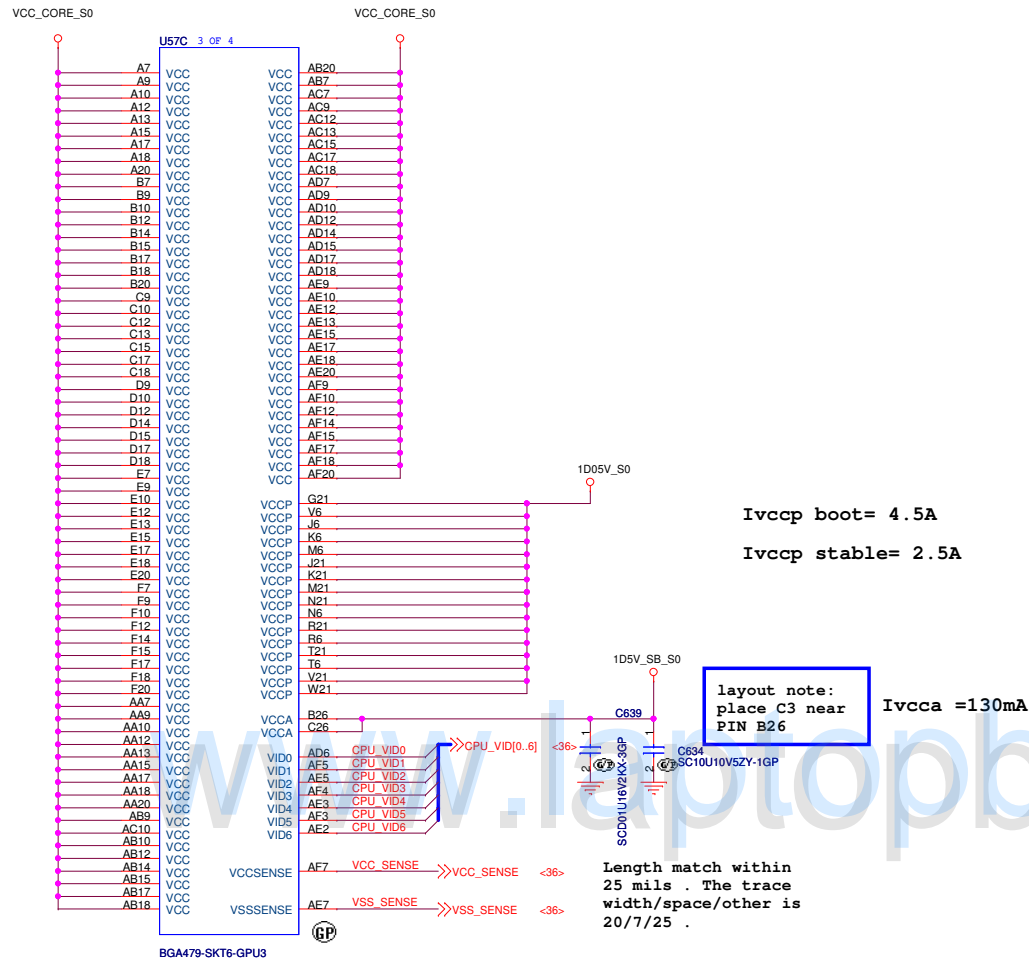


<8> H_A#[3..35

layout note: Zo = 55 ohm , 0.5" MAX for GTLREF

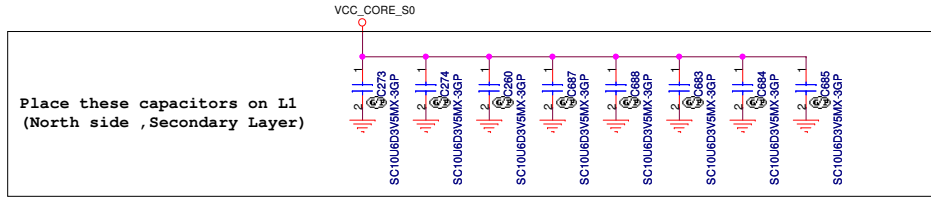
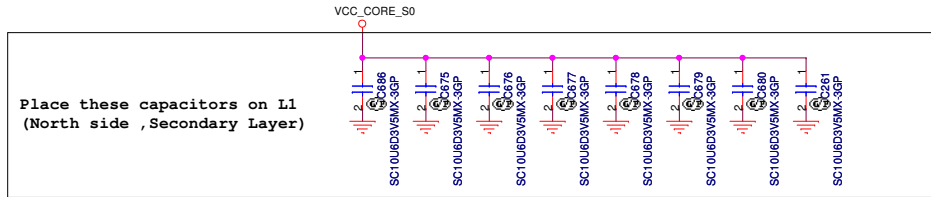
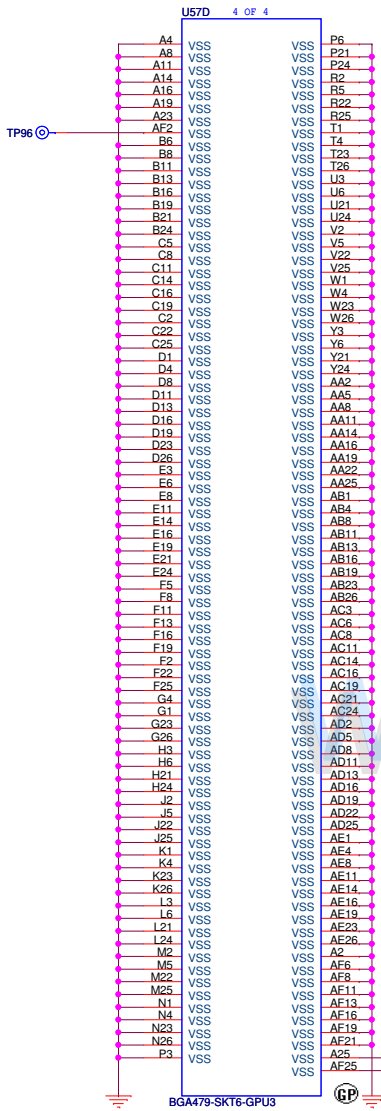


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

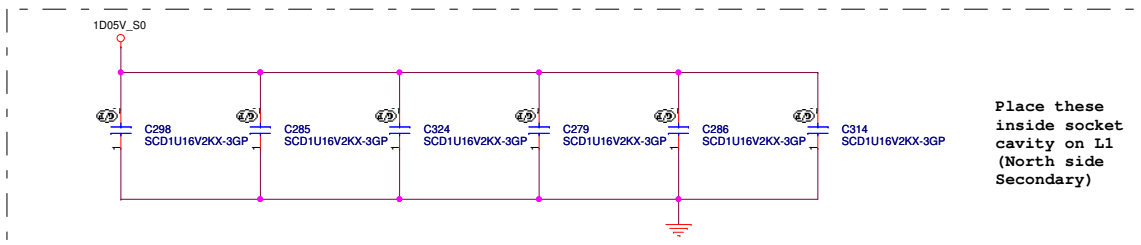
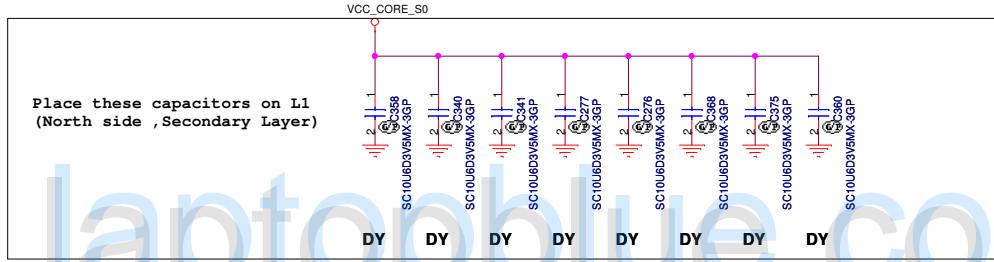


A-NOTE2

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Title	
Merom(2/3)-AGTL+/PWR	
Size A3	Document Number
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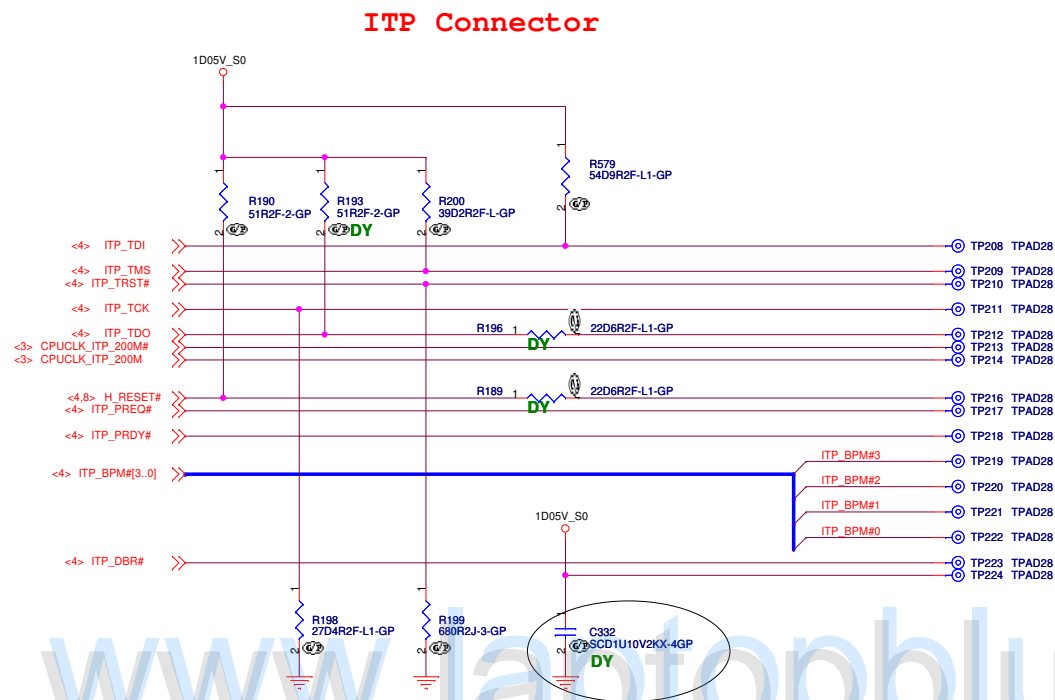


Mid Freqeuncd Decoupling



A-NOTE2

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Title		
Merom(3/3)-GND&Bypass		
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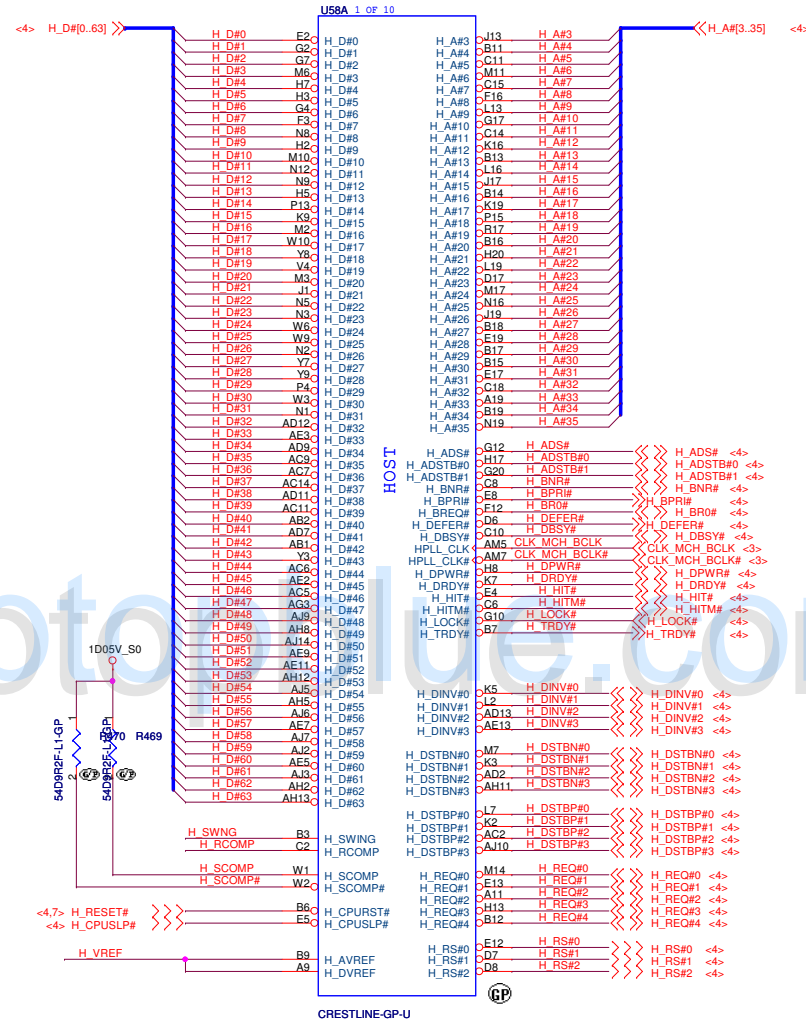
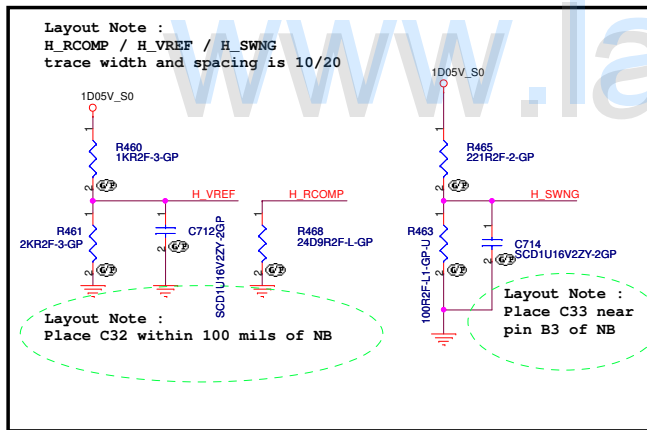


A-NOTE2

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Title			
Meron(3/3)-GND&Bypass			
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layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing
and impedance (55 ohm) same as FSB data traces

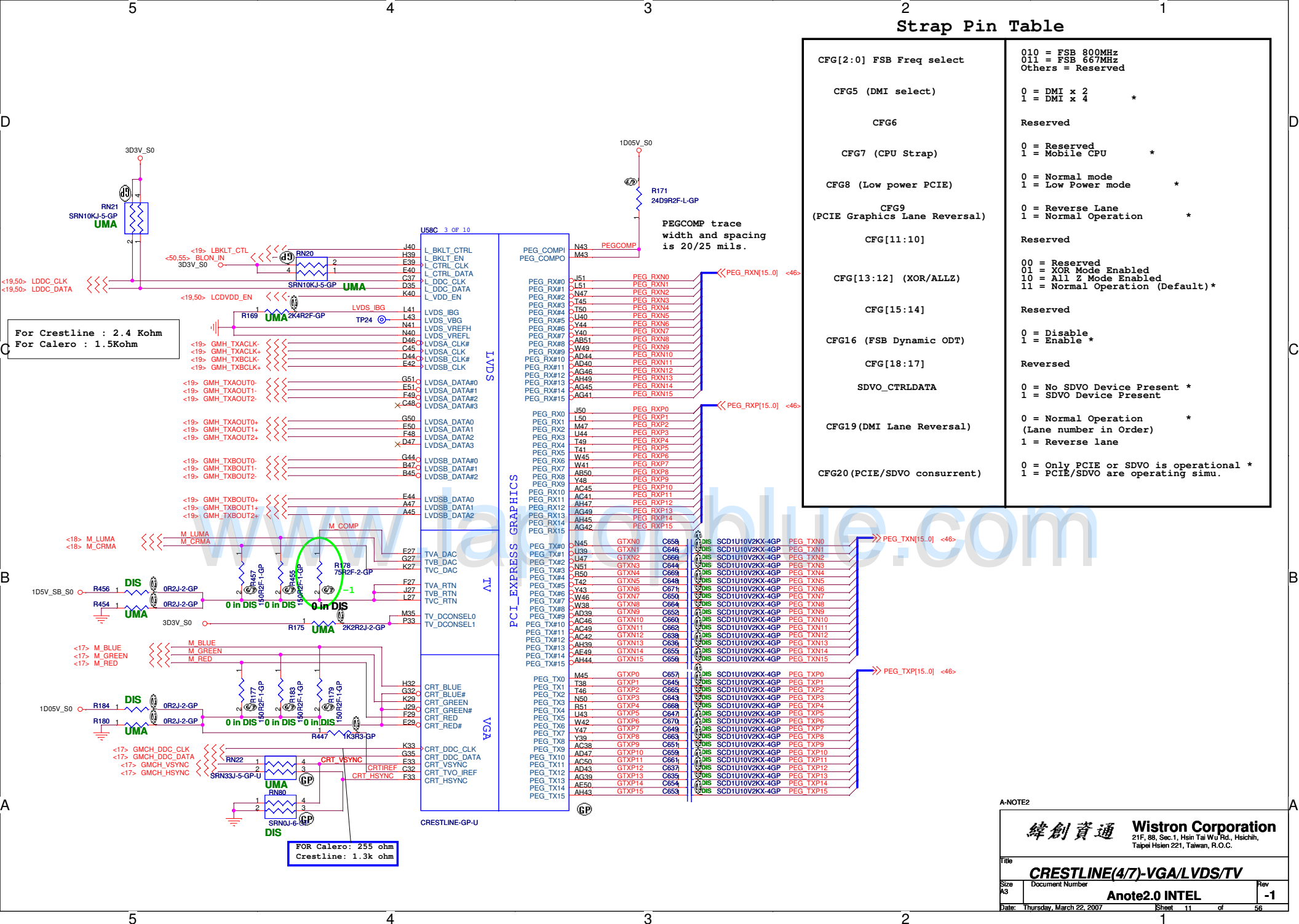
Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20



A-NOTE2

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Title CRESTLINE(1/7)-AGTL+/DM/DDR2
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Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse lane
CFG20(PCIE/SDVO consurent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

A-NOTE2

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Wistron Corporation

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Title

CRESTLINE(4/7)-VGA/LVDS/TV

Size

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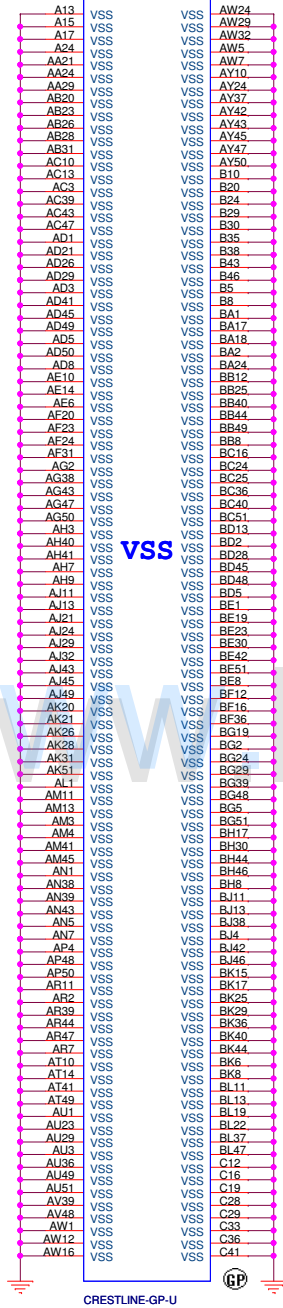
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Rev

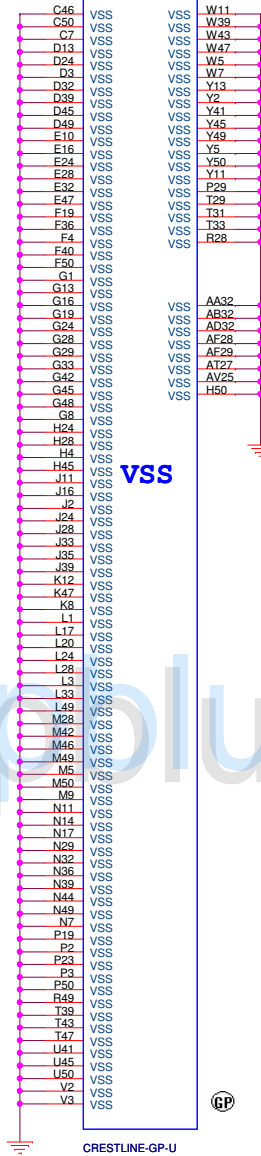
-1

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CRESTLINE-GP-U

U58J10 OF 10



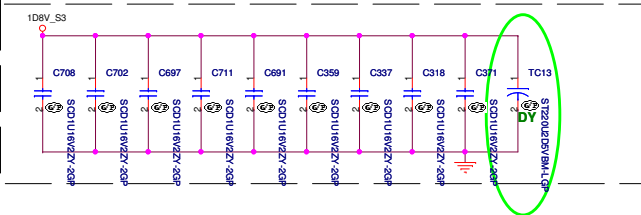
CRESTLINE-GP-U

A-NOTE2

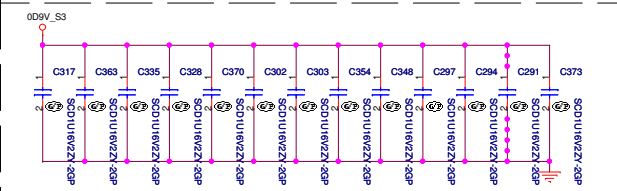
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CRESTLINE(7/7)-PWR/GND	
Size	Document Number
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<9> DDR_A_DQS[0..7] <<>>
 <9> DDR_A_DQ[0..63] <<>>
 <9> DDR_A_DM[0..7] <<>>
 <9> DDR_A_DQS[0..7] <<>>
 <9> DDR_A_MA[0..14] <<>>
 <9> DDR_A_BS[0..2] <<>>

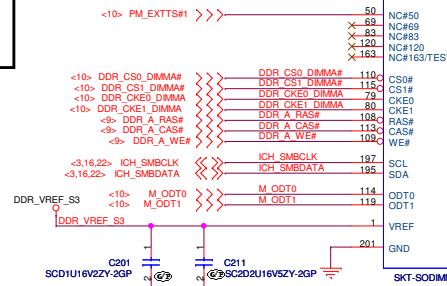
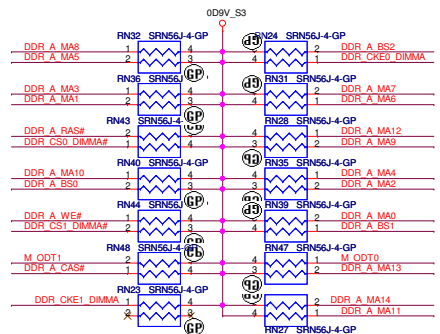
Layout Note:
Place near DM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors
closely DM1, all
trace length Max=1.5"

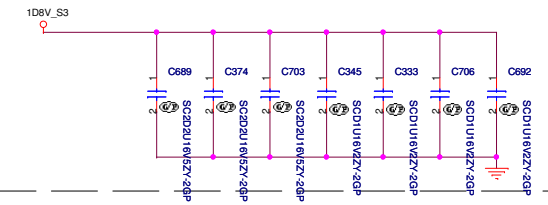


High 5.2mm

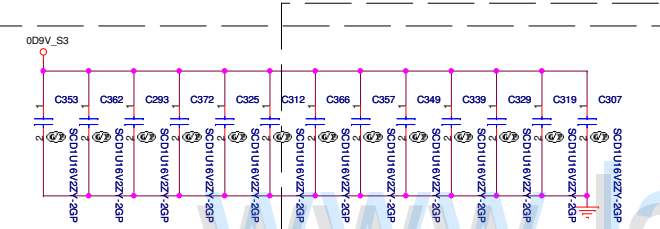
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 MH2
 MH2
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 DQS470 8990
 DQS471 9009
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 DQS474 9066
 DQS475 9085
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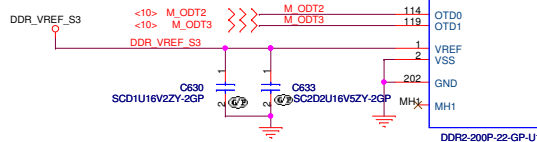
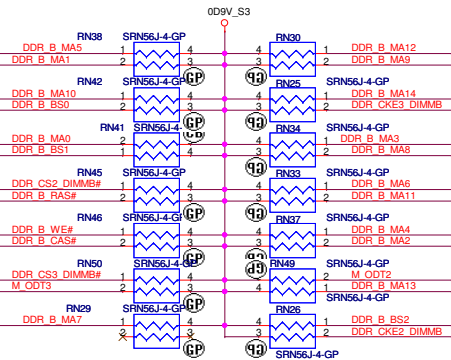
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistors
closely DM2, all
trace length Max=1.5"



62.10017.A61

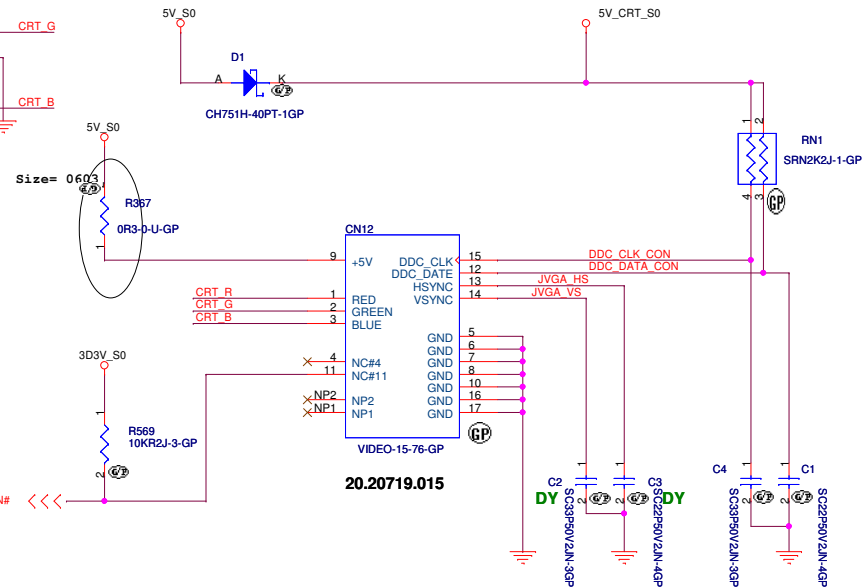
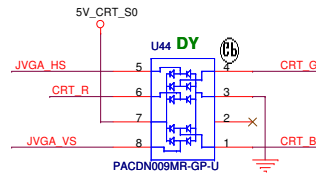
High 9.2mm
2nd source: 62.10017.A61

A-NOTE2

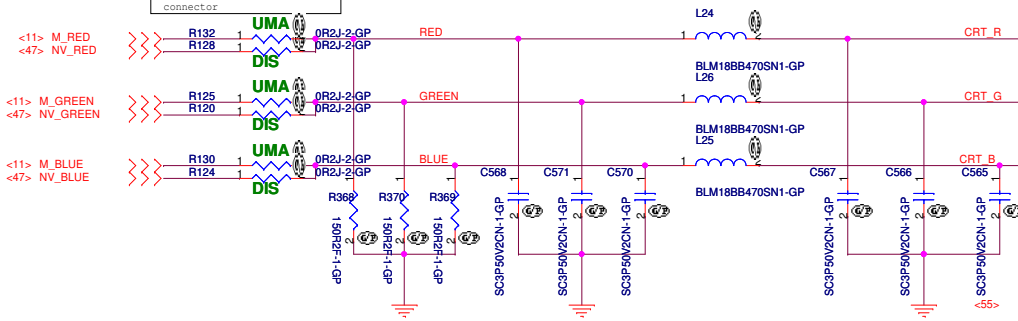
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tsu Wu Rd., Hsinchu,
Taippei Hsin 221, Taiwan, R.O.C.

Title	DDR2-SODIMM SLOT2	Rev	-1
Size	Document Number		
Custom	Anote2.0 INTEL		
Date	Thursday, March 22, 2007	Sheet	16 of 56

CRT I/F & CONNECTOR



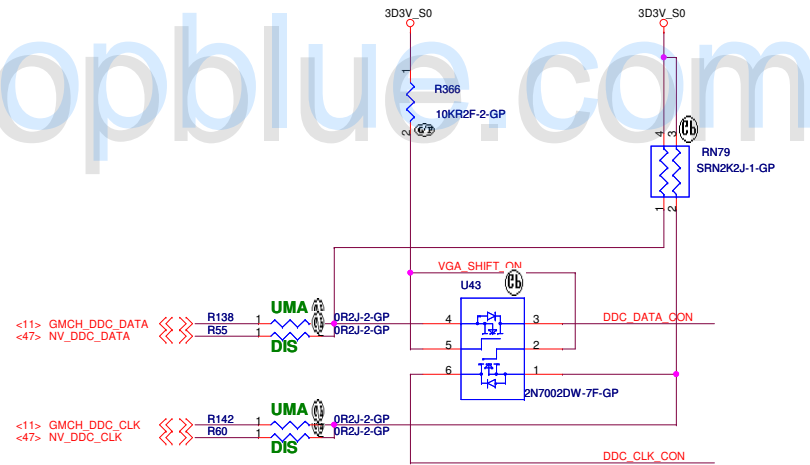
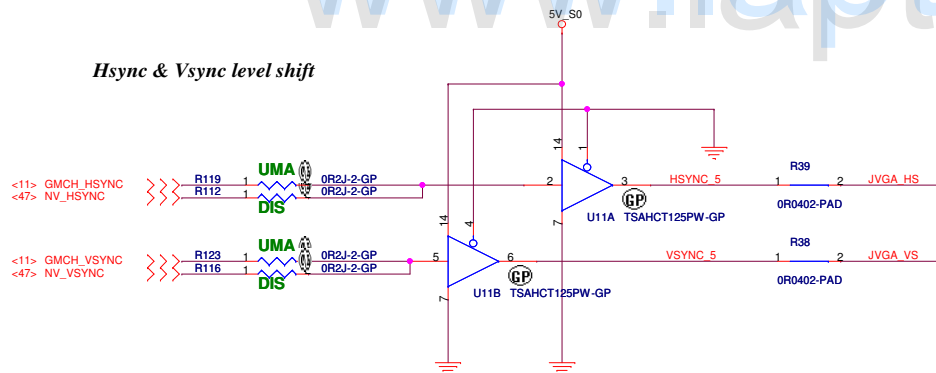
Layout Note:
Place these resistors
close to the CRT-out
connector



Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

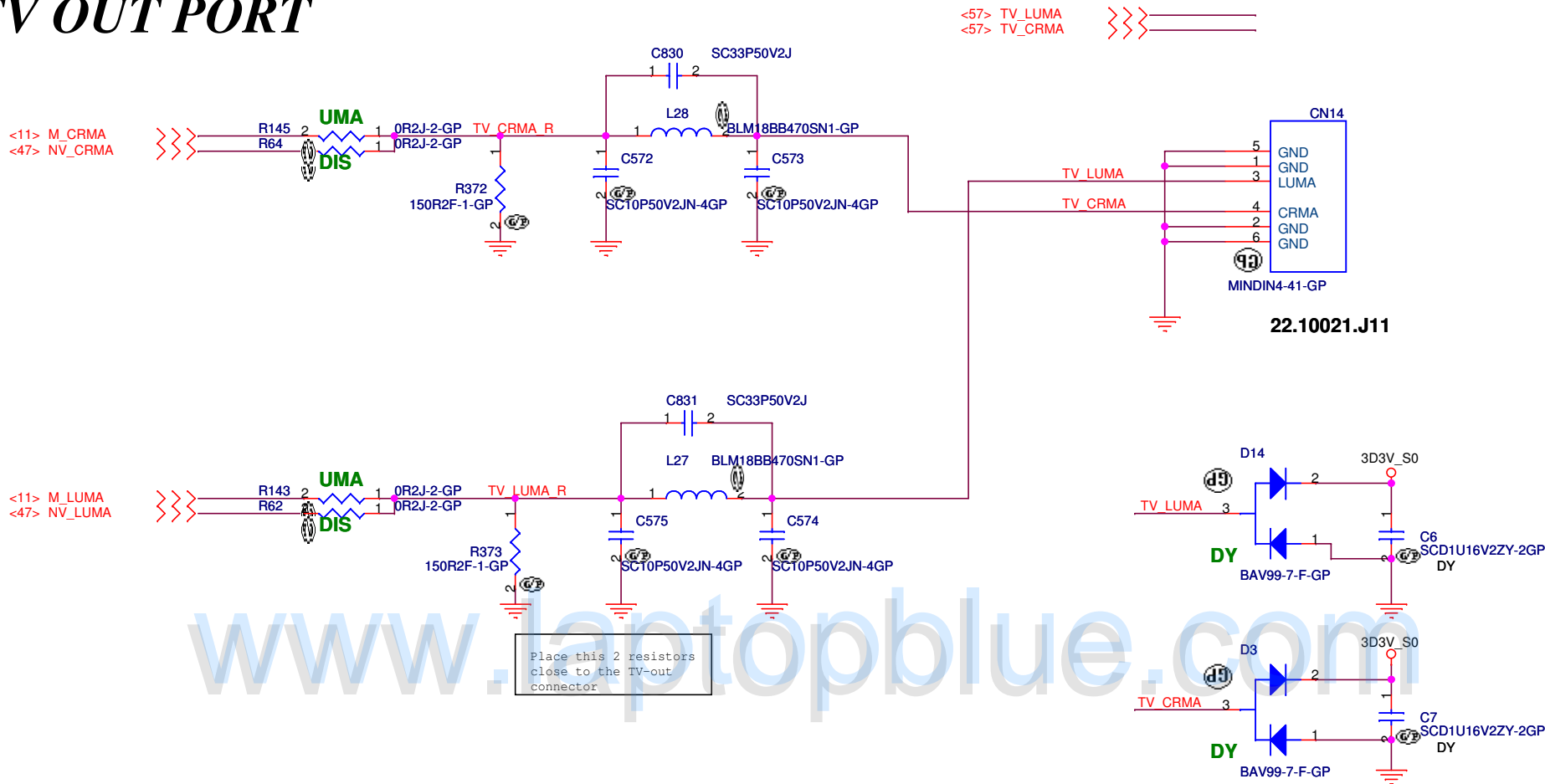


A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Connector		
Size A3	Document Number	Rev
	Anote2.0 INTEL	-1
Date: Thursday, March 22, 2007	Sheet 17	of 56

TV OUT PORT



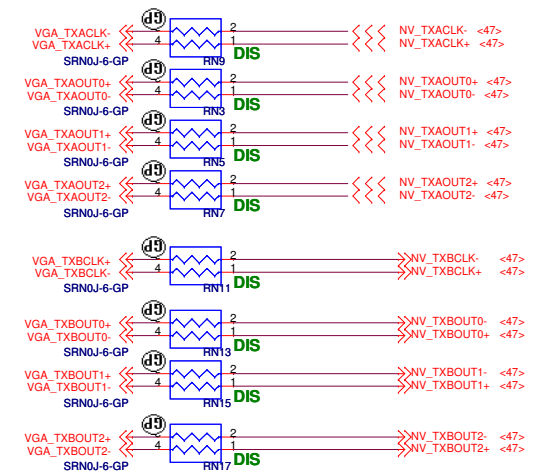
A-NOTE2

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TV Connector			
Size A4	Document Number Anote2.0 INTEL		Rev -1
Date:	Thursday, March 22, 2007	Sheet 18 of 56	

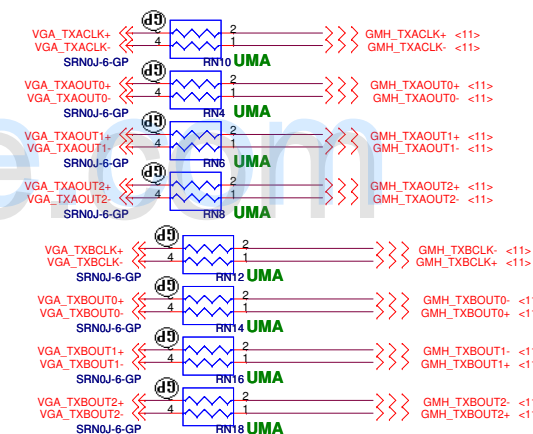
LED / INVERTER INTERFACE

LCD/INV CONN

ATI LVDS INTERFACE



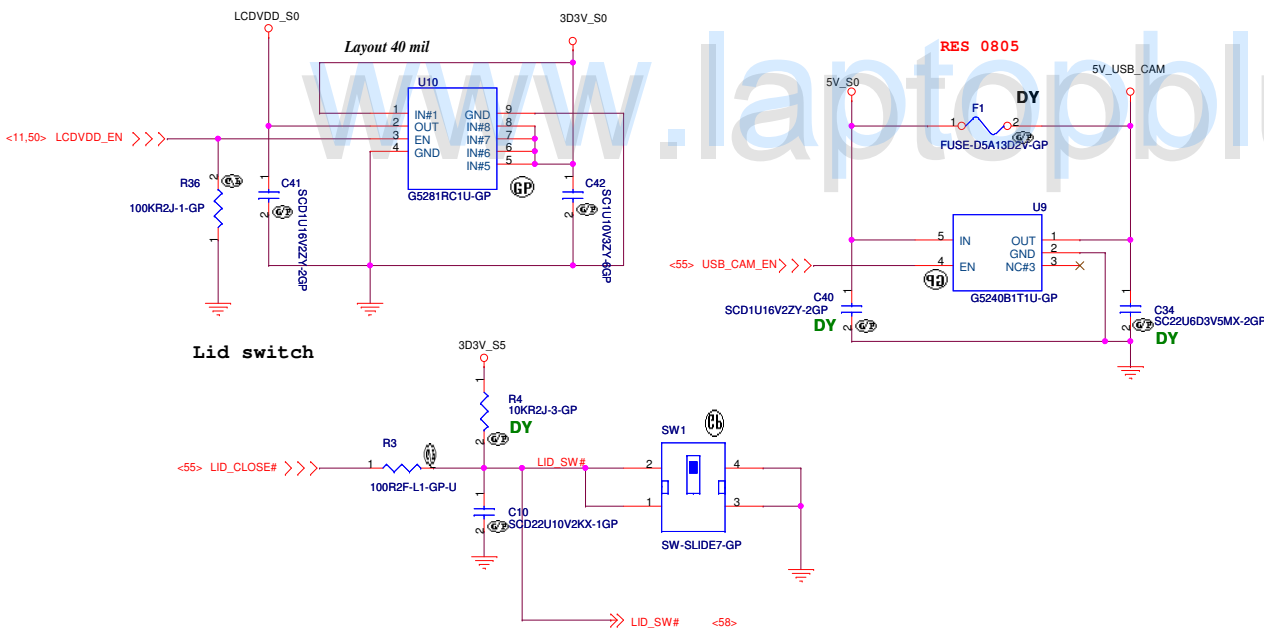
UMA LVDS INTERFACE

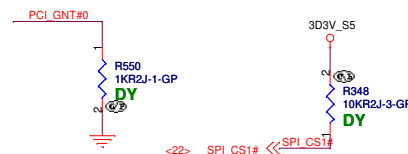
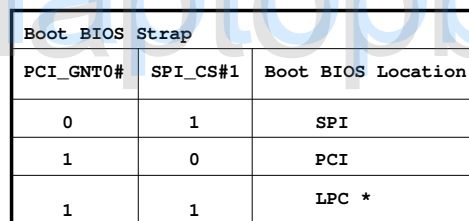
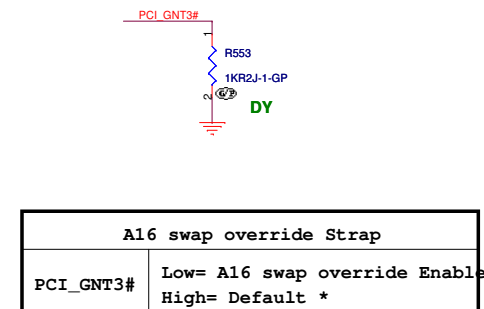


A-NOTE2

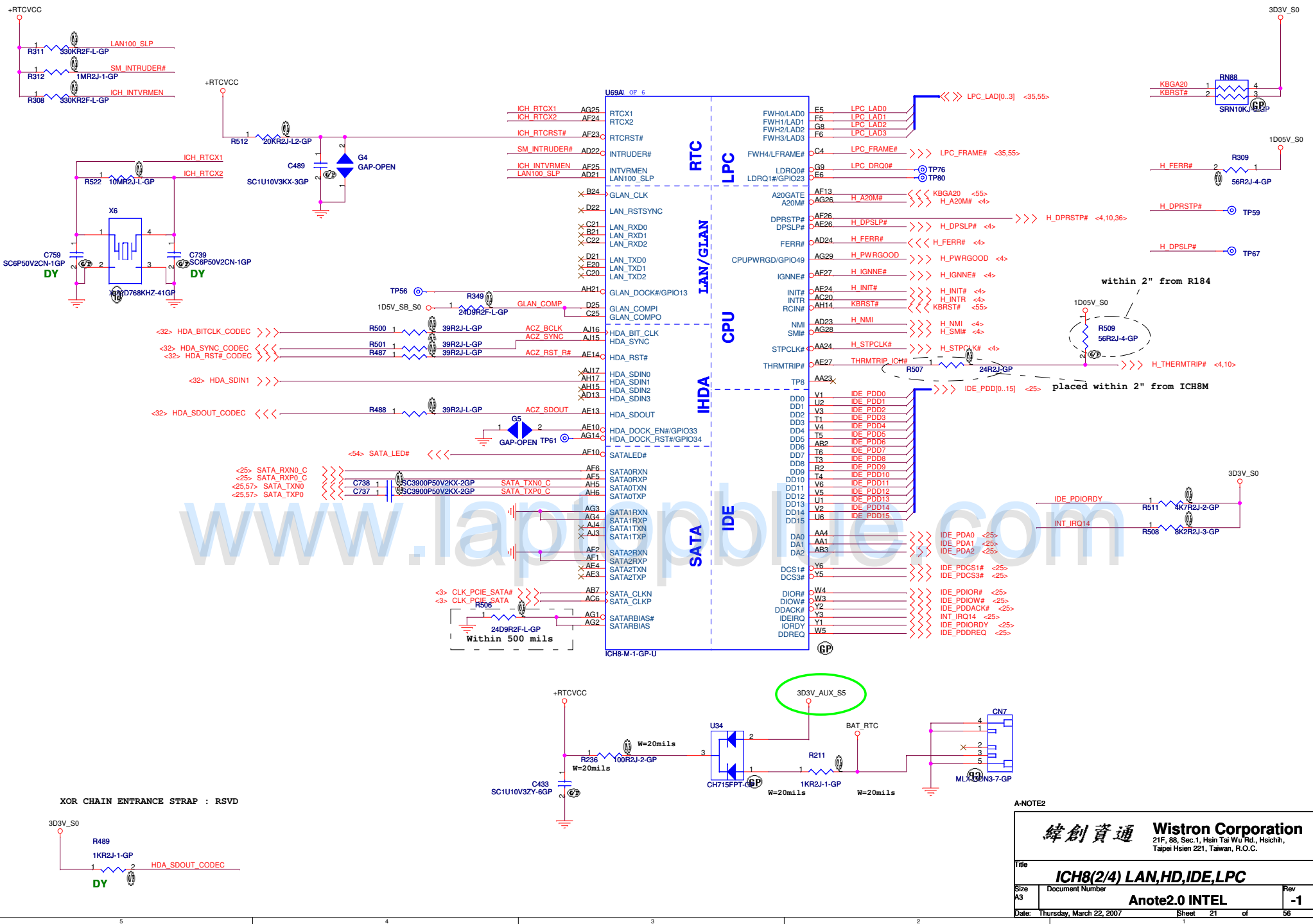
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

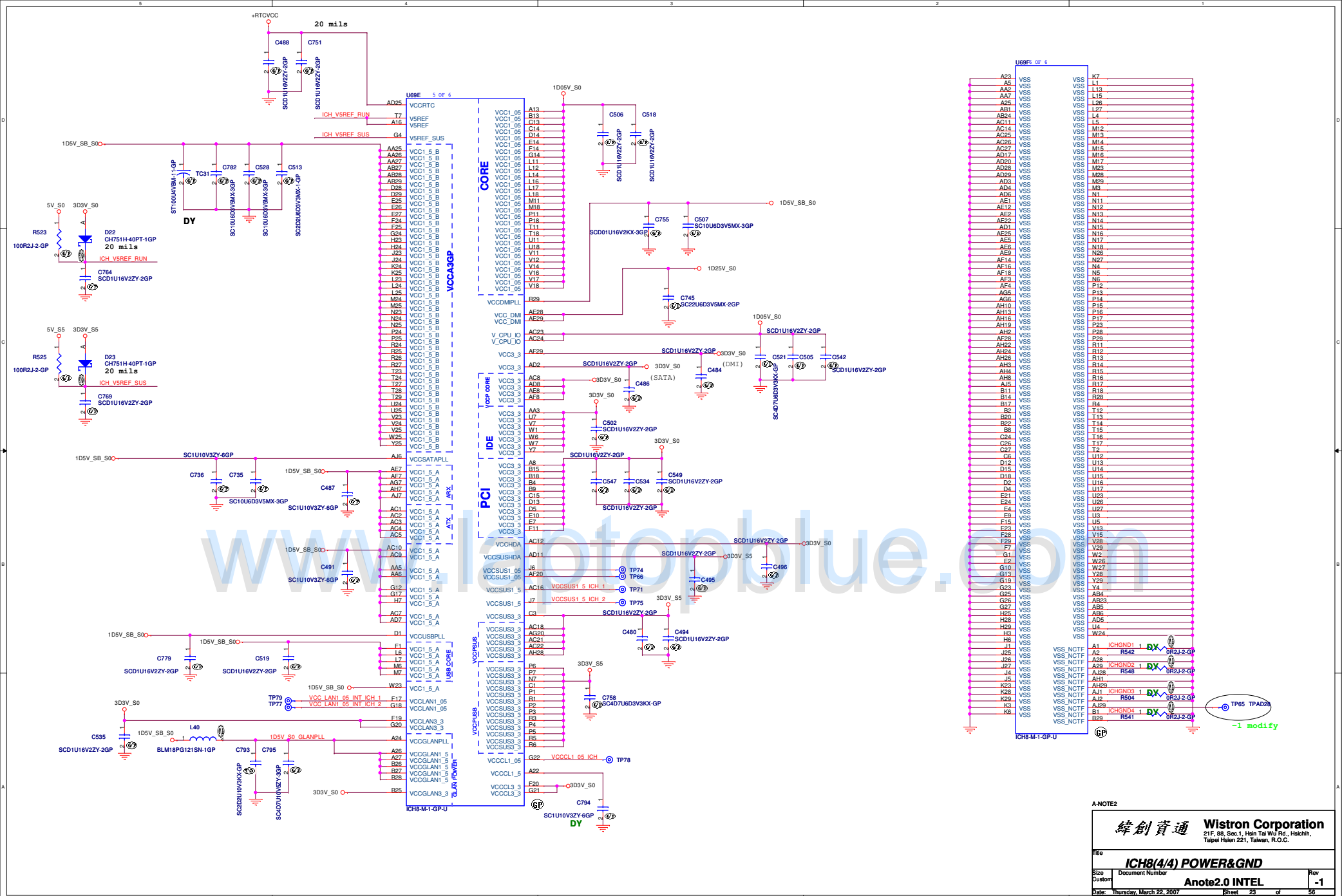
LCD/Inverter Connector			
Size A3	Document Number	Anote2.0 INTEL	
Date: Thursday, March 22, 2007	Sheet	19	of 56





Title			
ICH8(1/4)-PCI/INT			
Size A3	Document Number		Rev
	Anote2.0 INTEL		-1
Date:	Thursday, March 22, 2007	Sheet 20 of	56



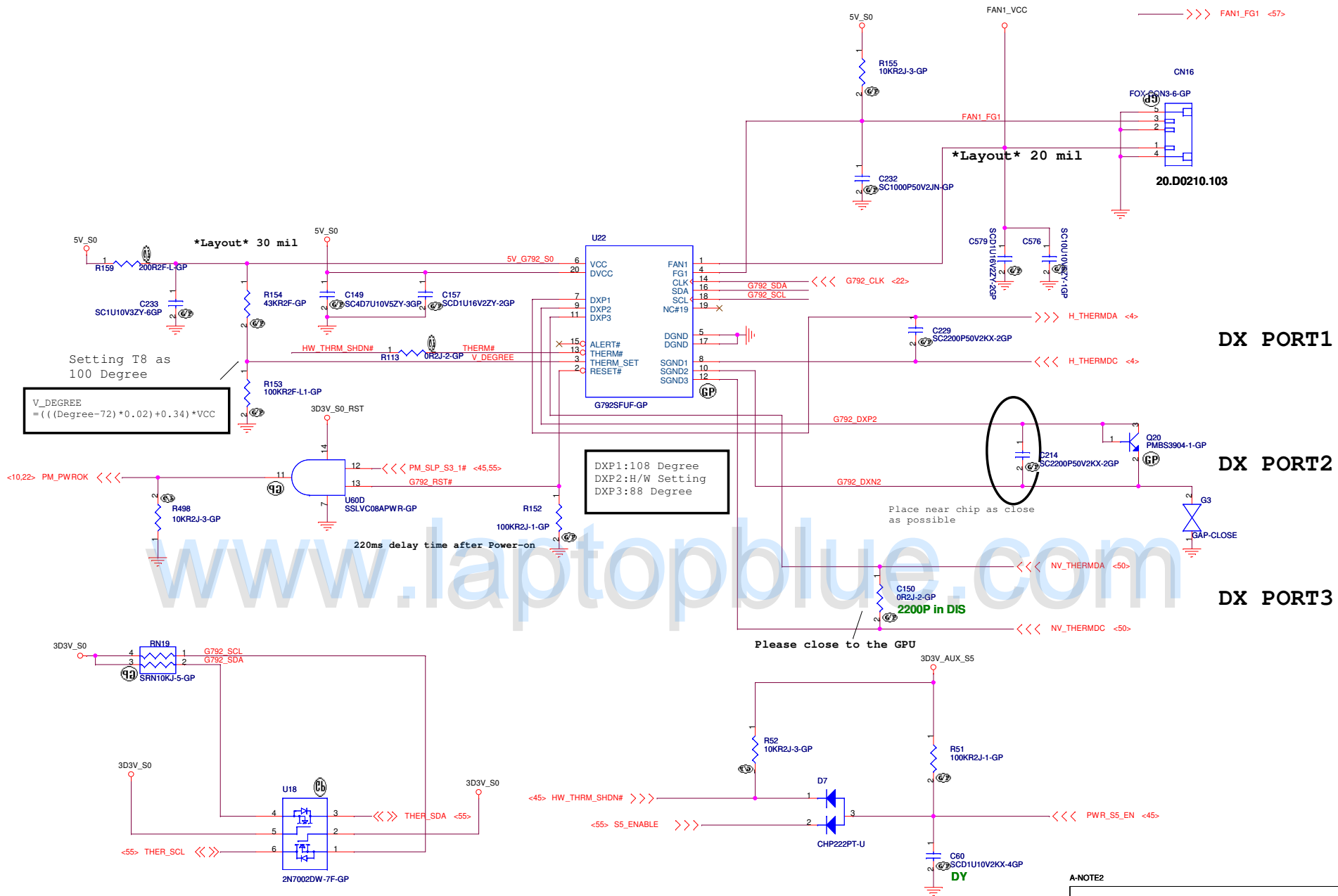


A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsueh-chi,
Taippei Hsien 221, Taiwan, R.O.C.

File: **ICH8(4/4) POWER&GND**
Size: Document Number
Custom: **Anote2.0 INTEL**
Date: Thursday, March 22, 2007 Sheet: 23 of 56

Rev: **-1**



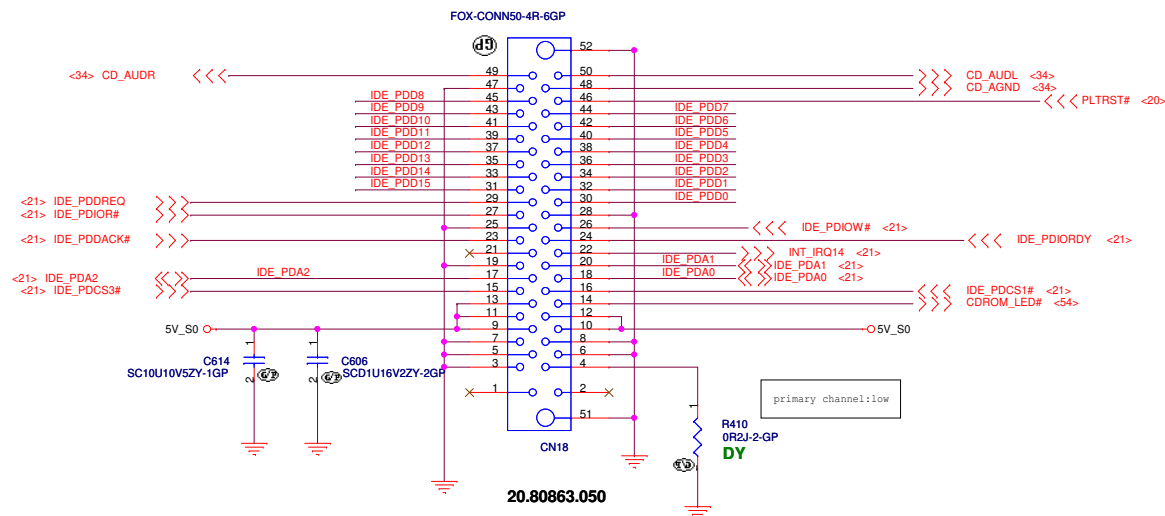
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Thermal/Fan Controller G792	
Size	Document Number
Custom	Anote2.0 INTEL
Date: Thursday, March 22, 2007	Sheet 24 of 56

CD-ROM CONNECTOR

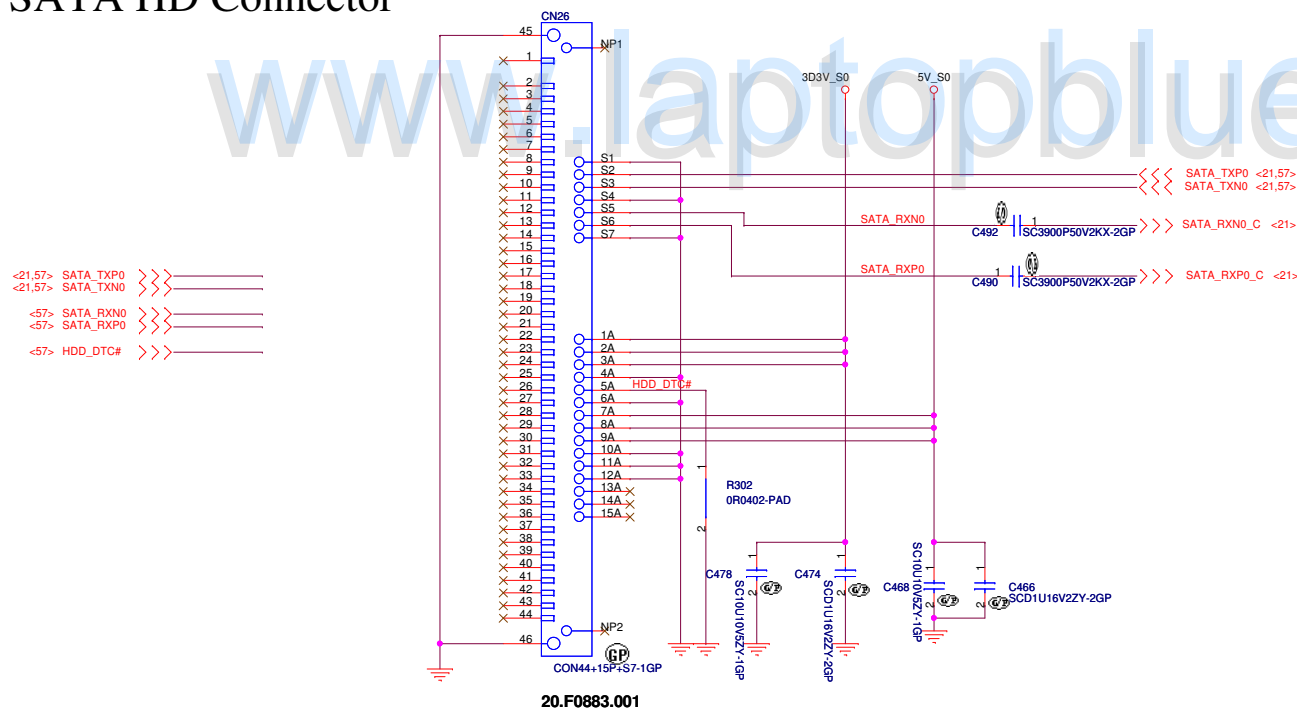
Lab1 20.80346.050

Lab2 20.80863.050

IDE_PDD[0..15] <21>



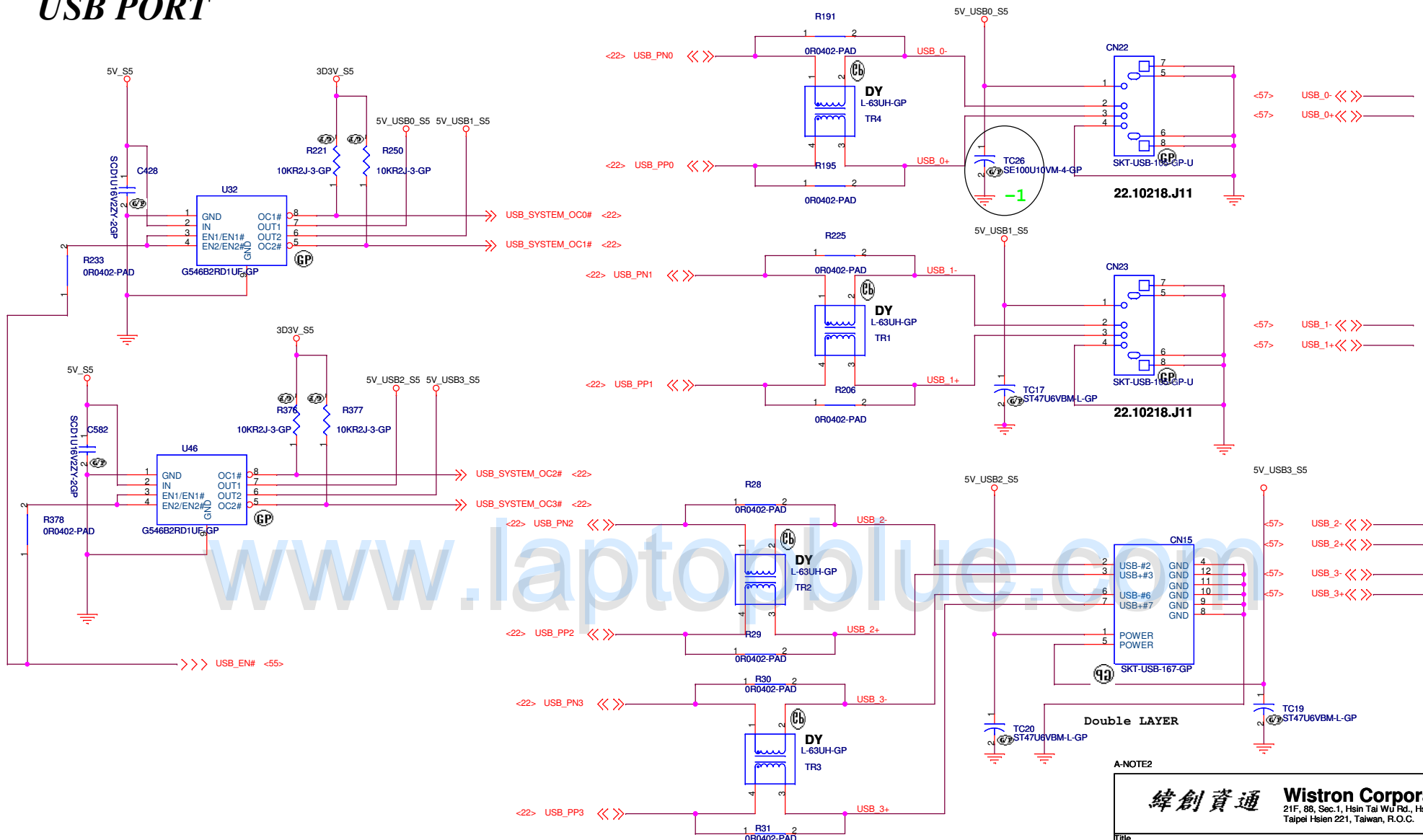
SATA HD Connector



A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
HD/CDROM/USB	
Title	Document Number
Size A3	Anote2.0 INTEL
Date: Thursday, March 22, 2007	Sheet 25 of 56
Rev -1	

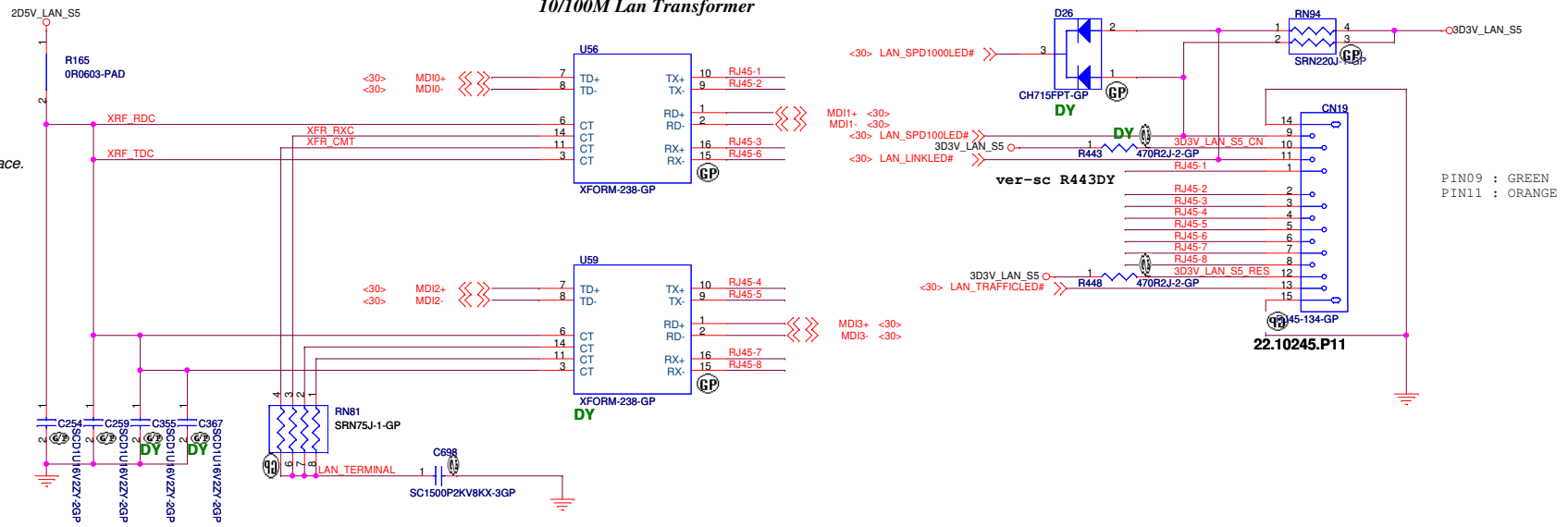
USB PORT



A-NOTE2

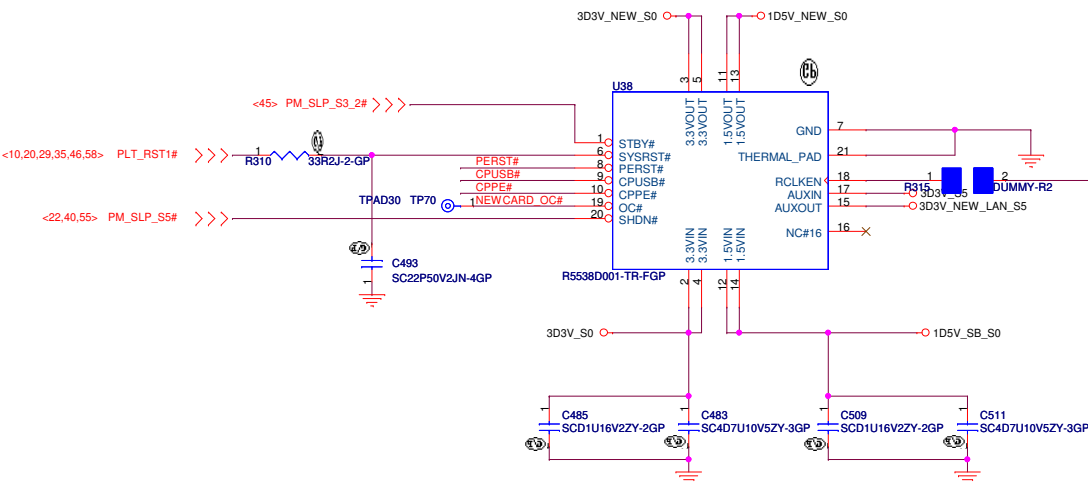
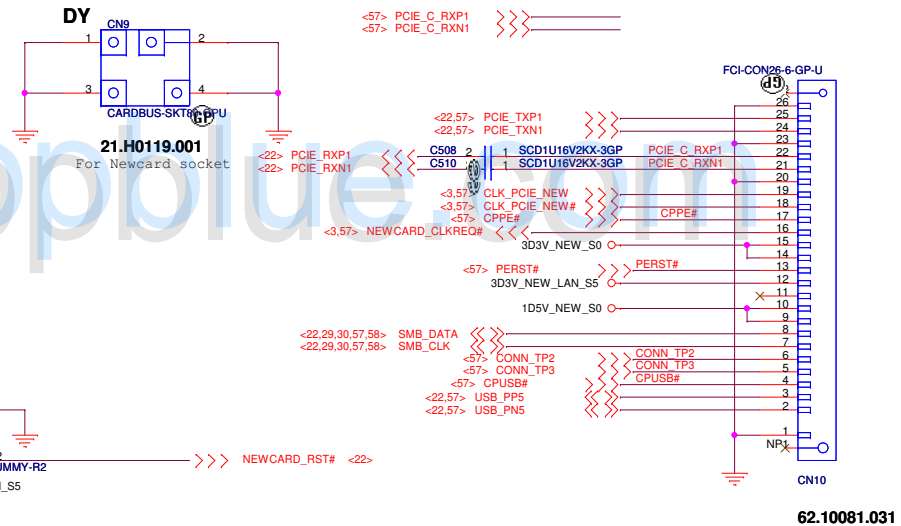
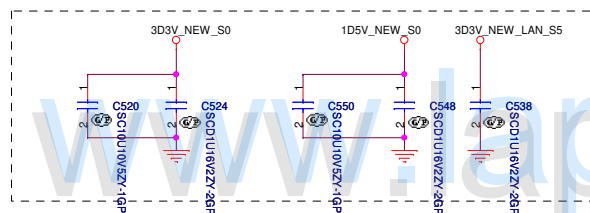
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB I/O	
Title Size B Date: Thursday, March 22, 2007	Document Number Anote2.0 INTEL Sheet 26 of 56
Rev -1	

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



Place them Near to Chip

Place them Near to Connector



A-NOTE2

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

LAN connector/NEW CARD/SIM

Anote2.0 INTEL

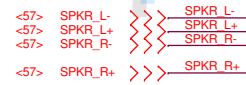
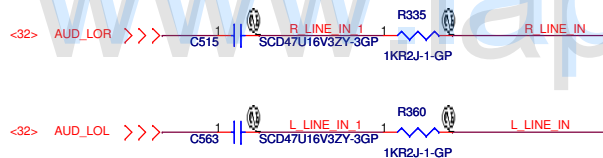
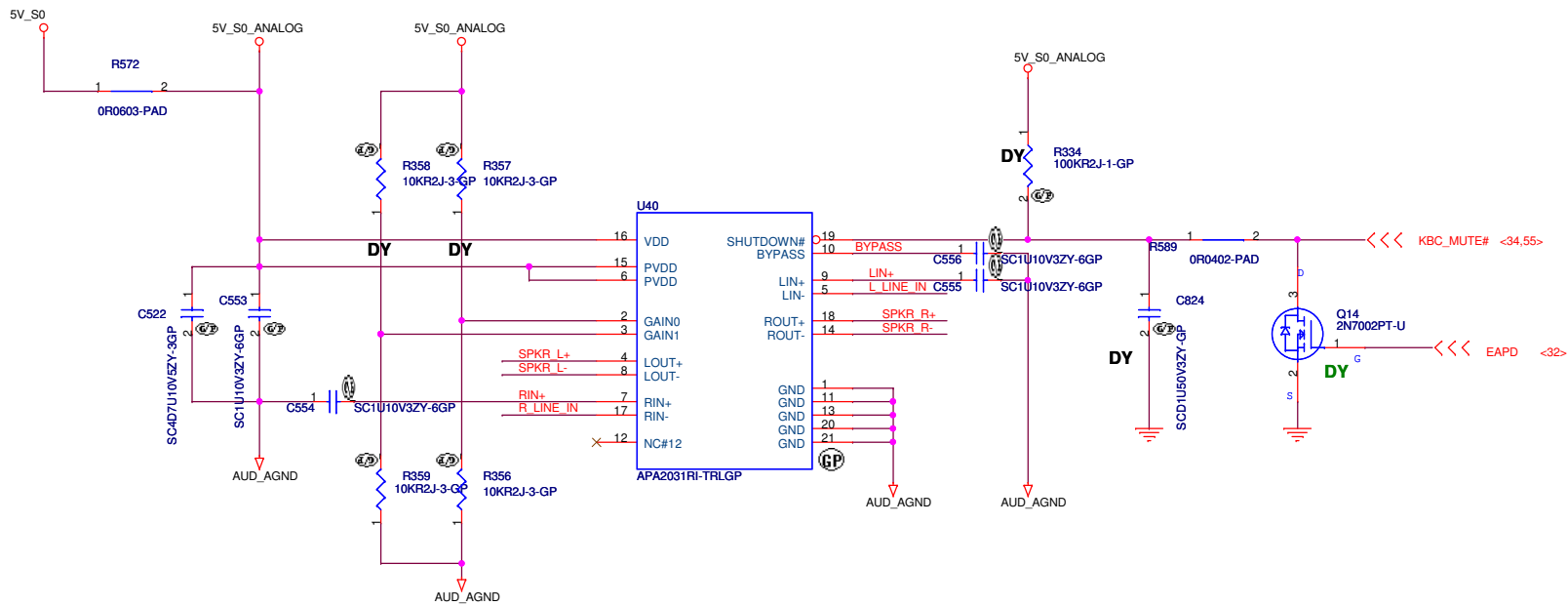
Rev

Date: Thursday, March 22, 2007

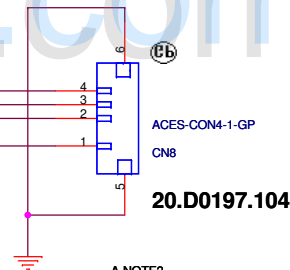
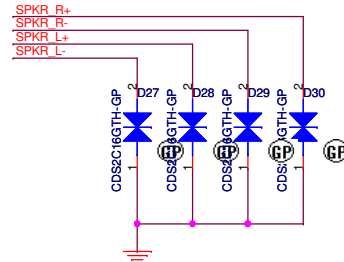
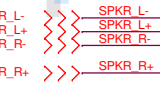
Sheet 3

E

6



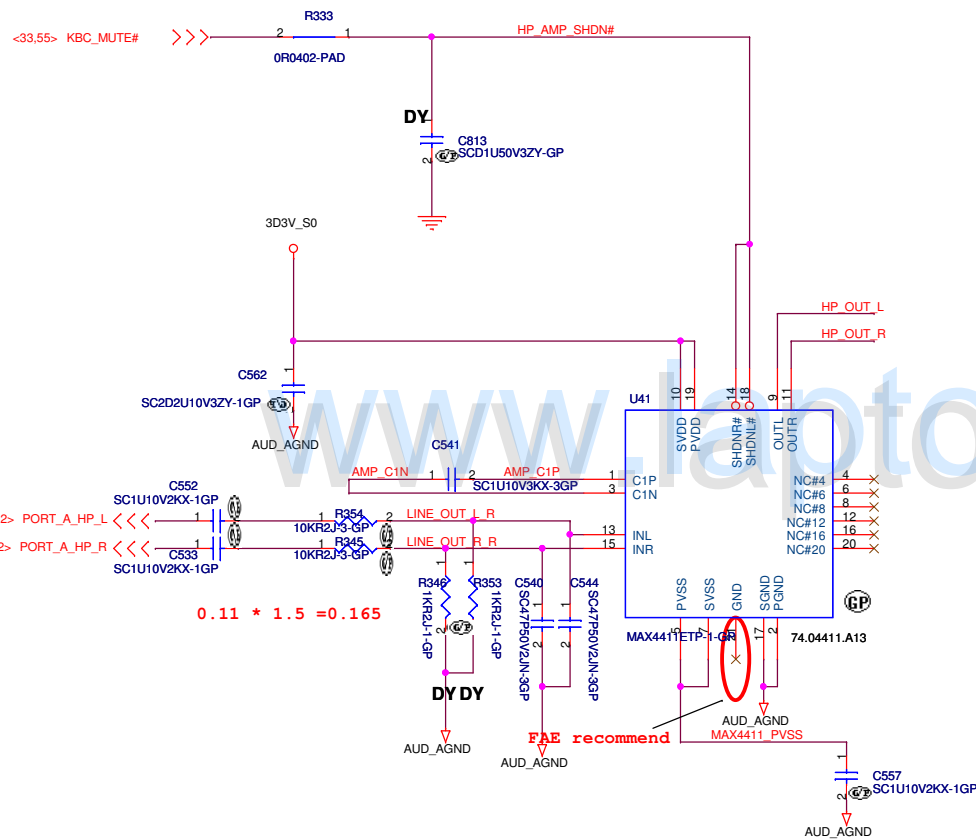
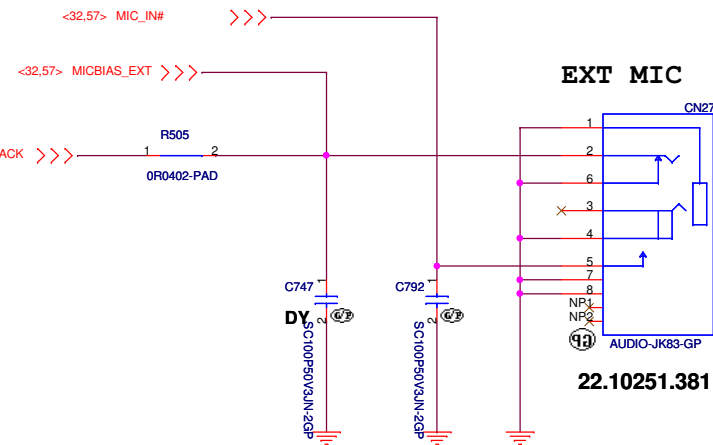
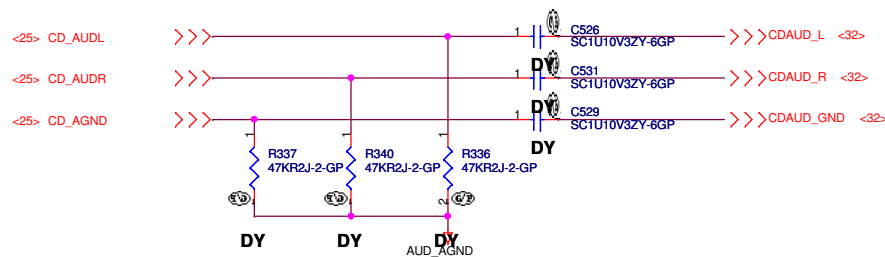
Speaker



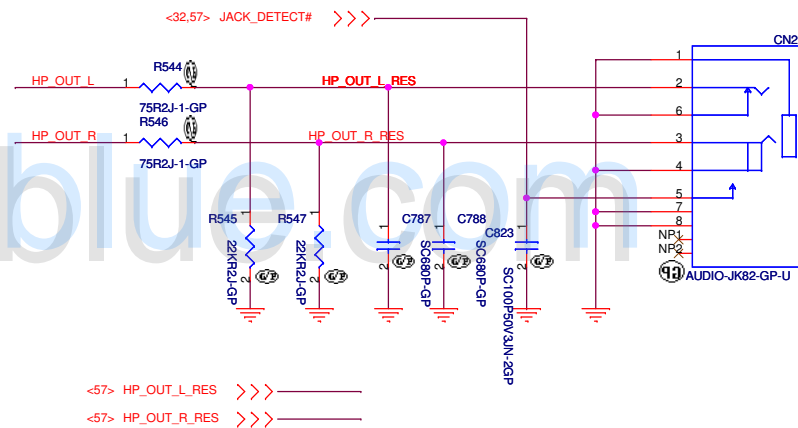
A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title AUDIO AMP/SPEAKER	
Size B	Document Number Anote2.0 INTEL
Date: Thursday, March 22, 2007	Rev -1

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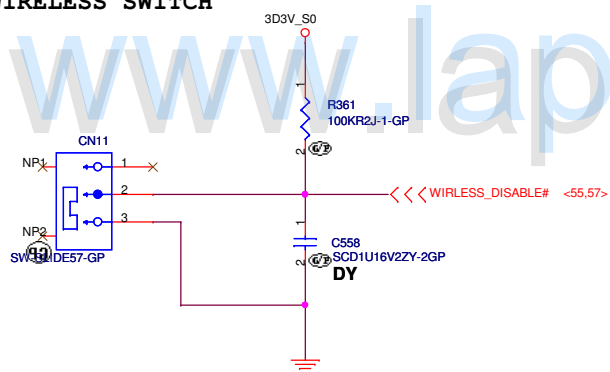
HP_OUT/ LINE_OUT



A-NOTE2

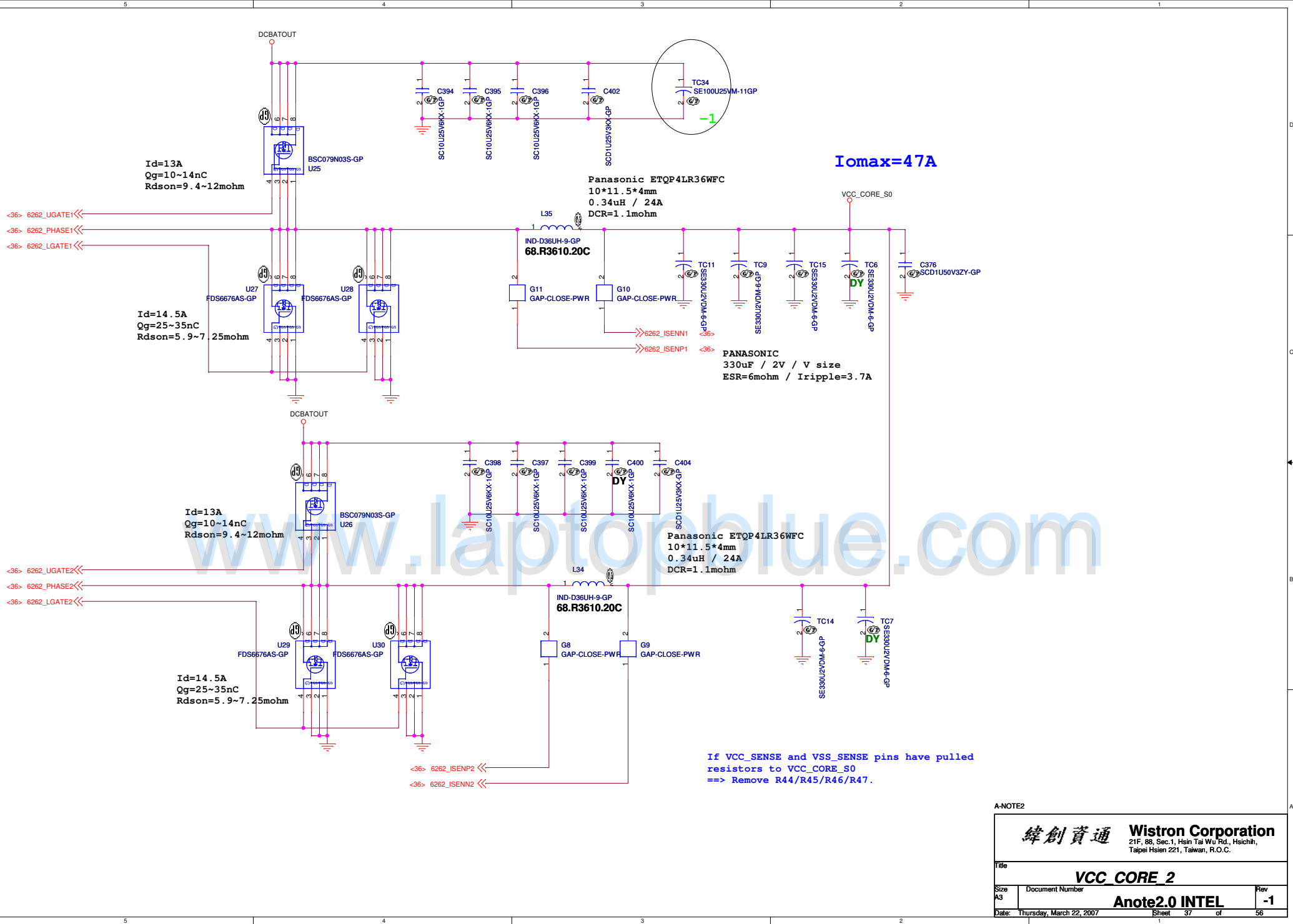
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
AUDIO HP_JK/ MIC_JK	
Title	Document Number
Size B	Anote2.0 INTEL
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Rev	-1

GOLDEN FINGER FOR DEBUG BOARD



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

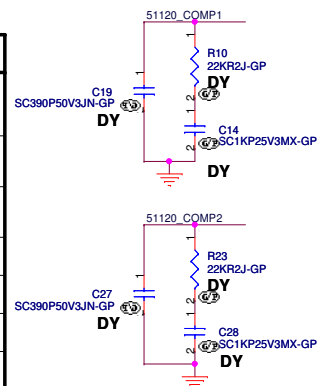
Title			
<i>FWH and Debug</i>			
Size B	Document Number	Anote2.0 INTEL	Rev -1
Date: Thursday, March 22, 2007	Sheet 35	of	56



A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
VCC CORE 2	
Title Size A3 Date: Thursday, March 22, 2007	Document Number Anote2.0 INTEL Sheet 37 of 56
Rev -1	

Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	5V fixed output Adjustable output (connect to the resistor divider)			
VFB2	3.3V fixed output Adjustable output (connect to the resistor divider)			
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)



$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120,
Vout=5V

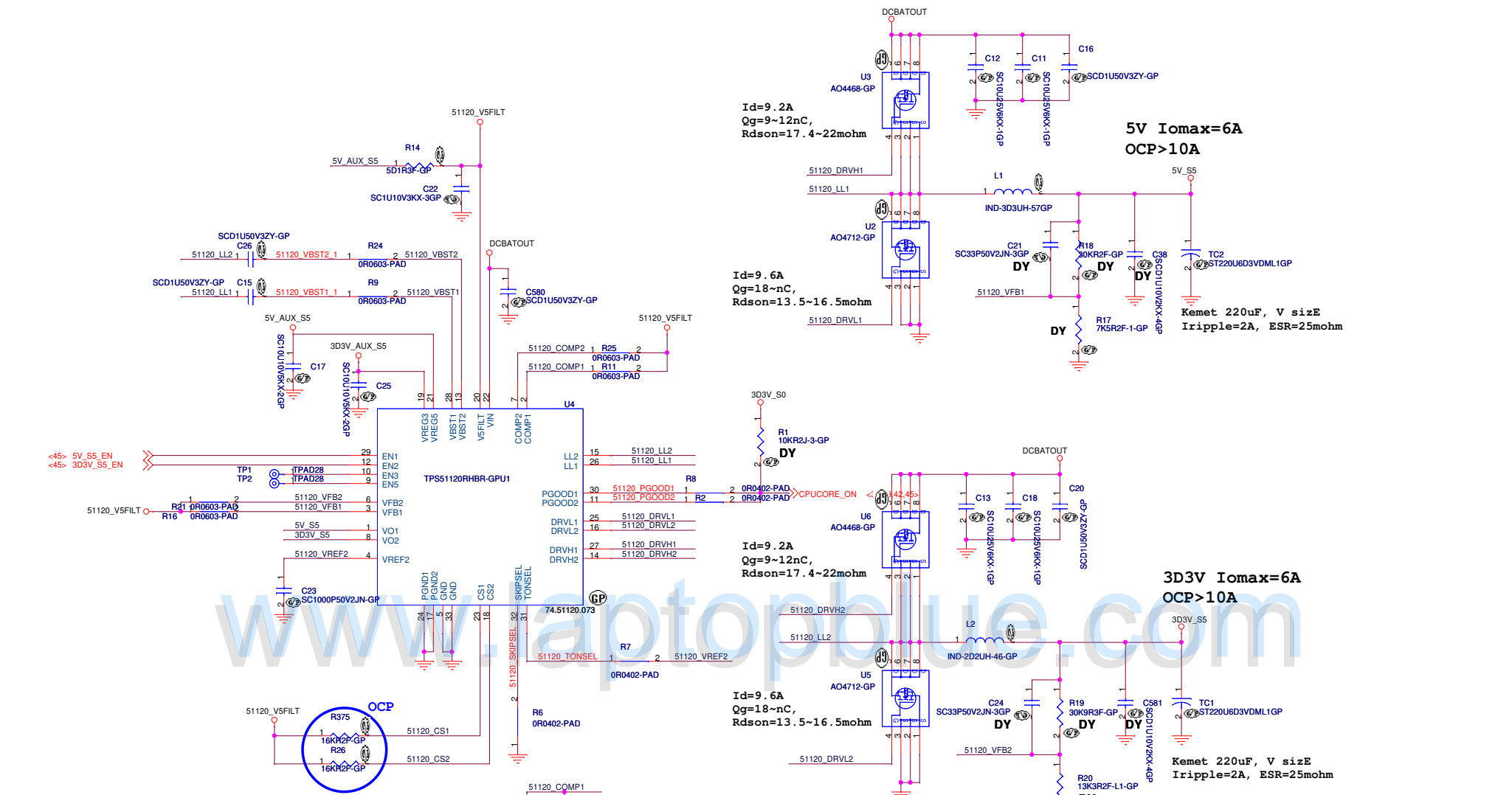
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
 2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
 3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
- Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
 2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
 3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

A-NOTE2

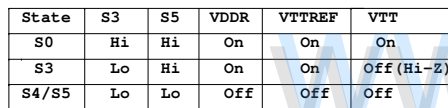
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	TPS51120 5V / 3D3V
Size	Document Number
A3	Anote2.0 INTEL
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Rev

-1

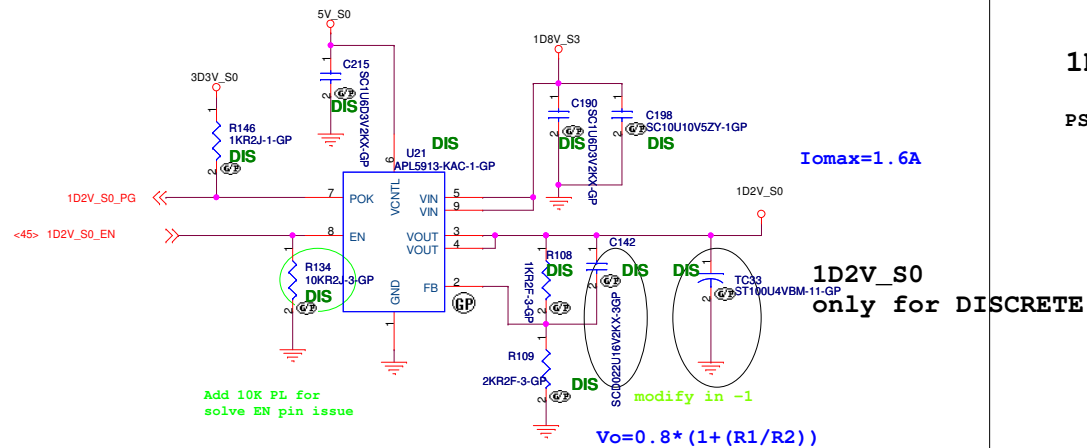


Forum
LAPTOPBLUE.VN



Title			
TPS51116 1D8V/0D9V			
Size A3	Document Number	Anote.2.0 INTEL	Rev -1
Date: Thursday, March 22, 2007	Sheet 40	of 56	

VGA 1.2V Power

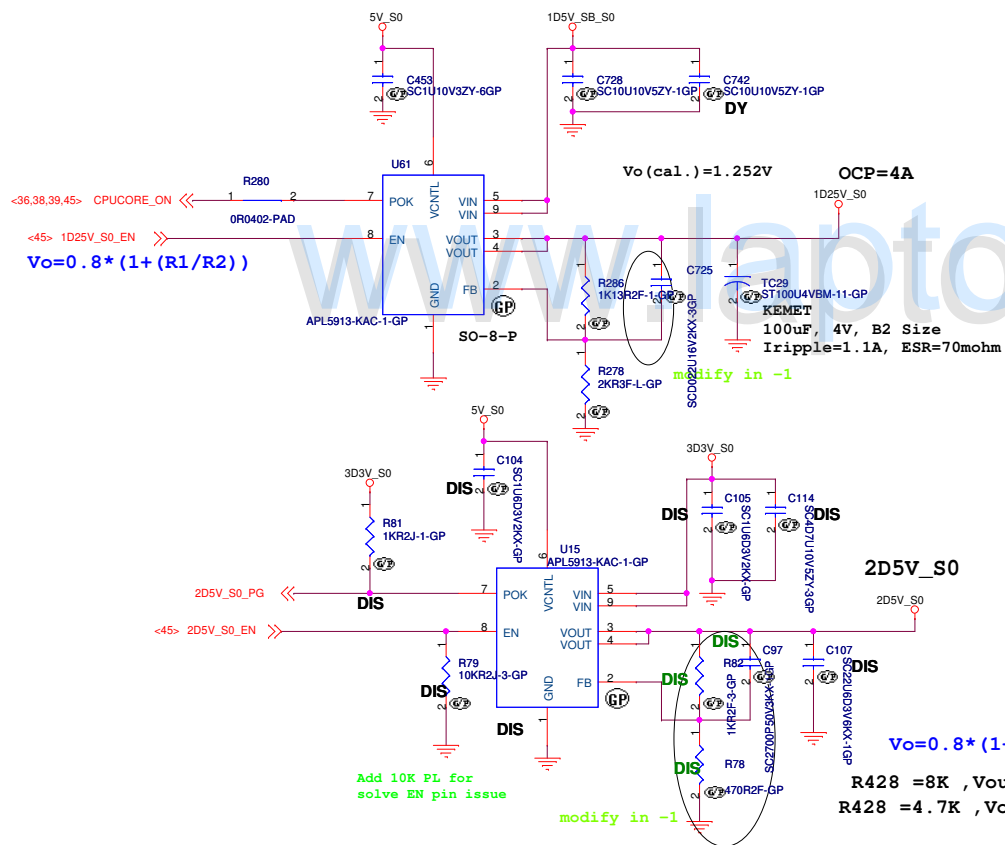


1D5V_NB

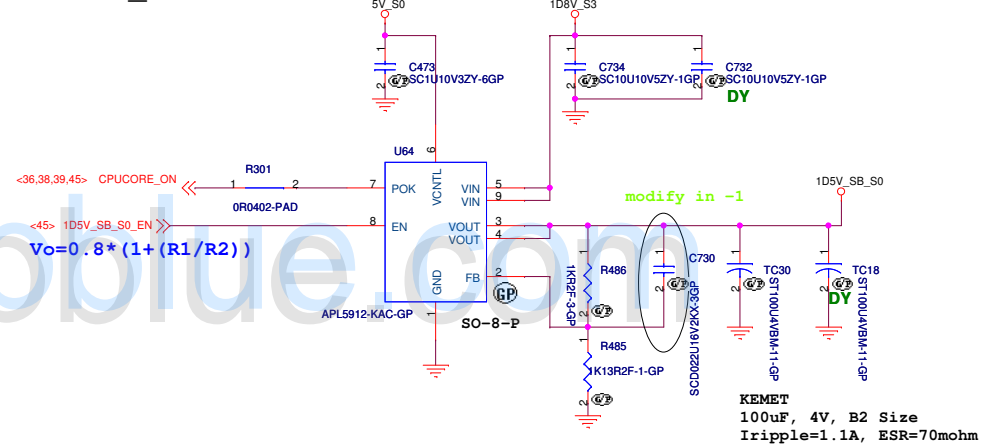
PS: SB del

1D25V_S0

Iomax=2.0A



1D5V_SB

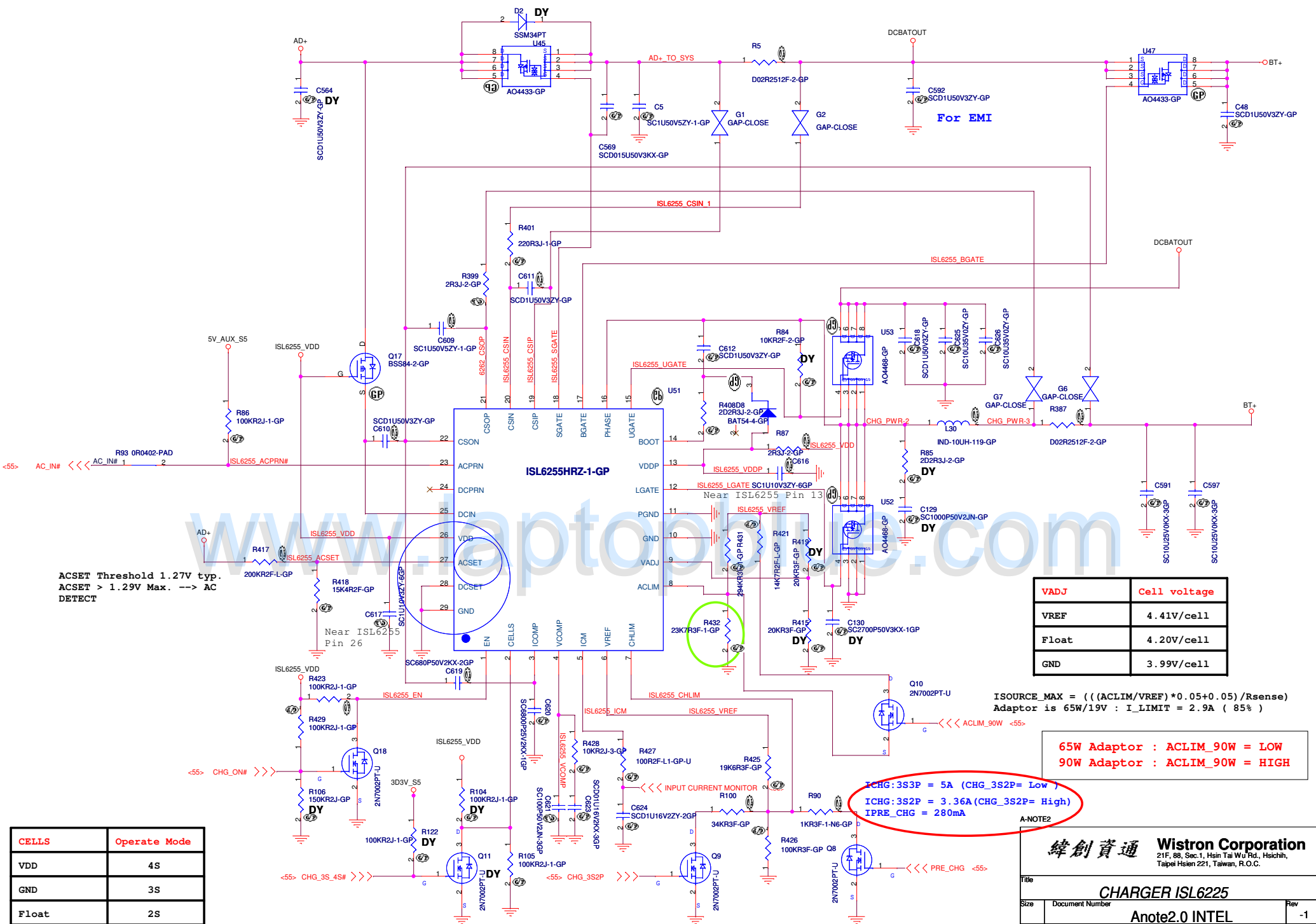


2D5V_S0 only for DISCRETE

A-NOTE2

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
1D2V_VGA/2D5V/1D25V/1D5V LDO		
Size	Document Number	Rev
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CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE_MAX = ((ACLIM/VREF)*0.05+0.05)/Rsense
 Adaptor is 65W/19V : I_LIMIT = 2.9A (85%)

65W Adaptor : ACLIM_90W = LOW
 90W Adaptor : ACLIM_90W = HIGH

ICHG:3S3P = 5A (CHG_3S2P= Low)
 ICHG:3S2P = 3.36A(CHG_3S2P= High)
 IPRE_CHG = 280mA

A-NOTE2

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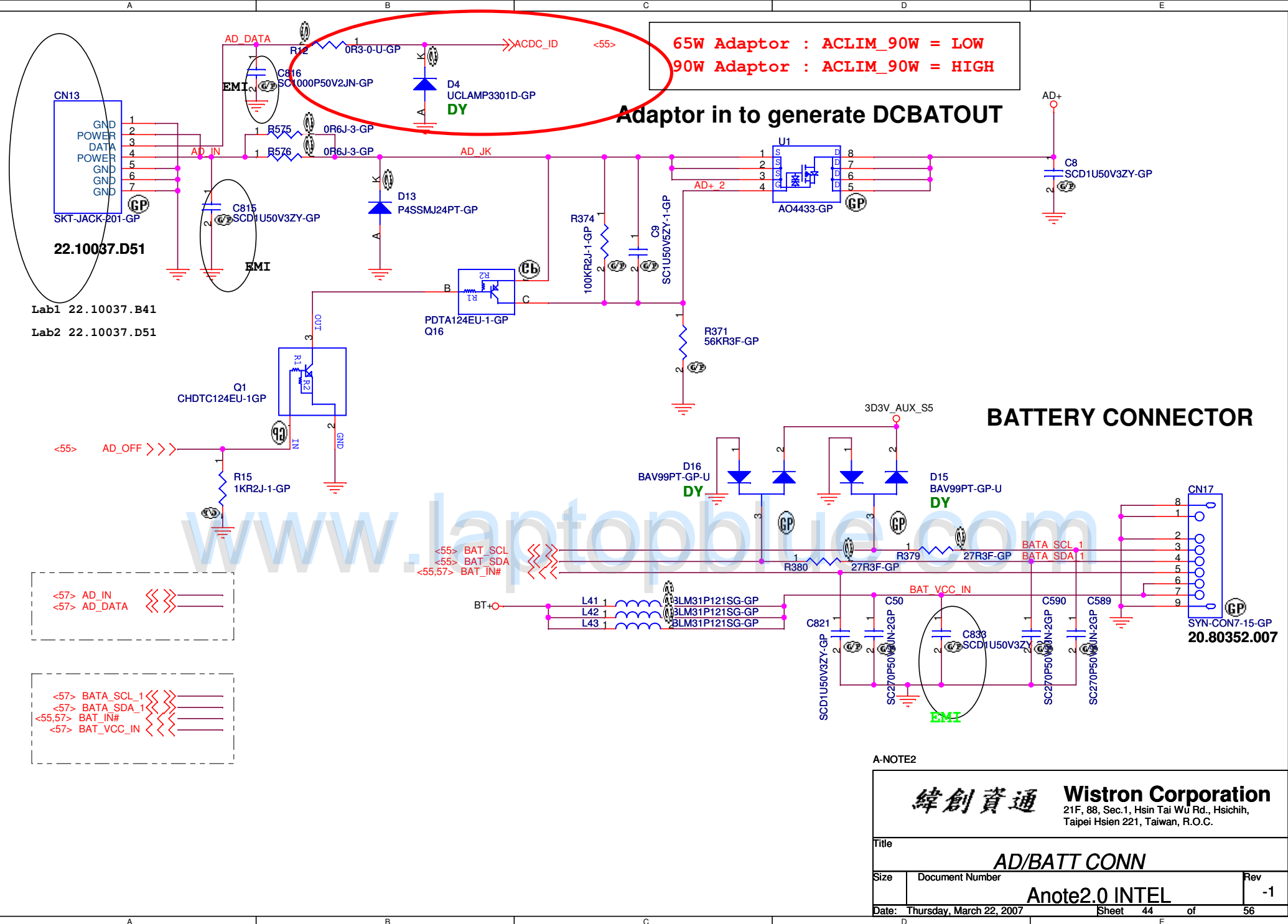
Title: **CHARGER ISL6225**

Size: Document Number

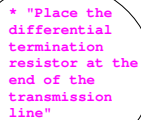
Date: Thursday, March 22, 2007

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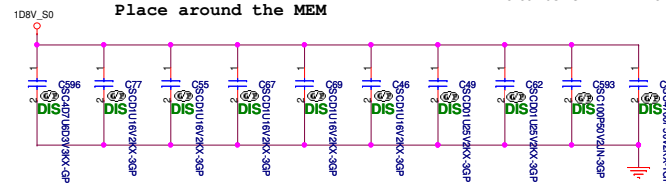
Rev -1



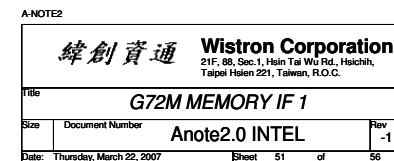




Decoupling for right MEMORY
Place around the MEM



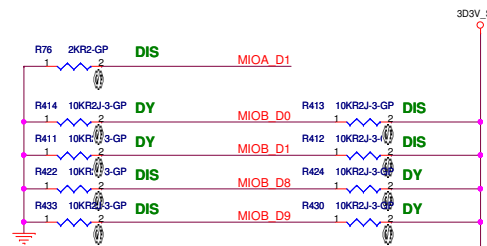
Title				G72M VRAM (1ST 1/2)			
Size		Document Number				Rev	
		Anoto2.0 INTEL				-1	
Date:		Thursday, March 22, 2007		Sheet		48 of 56	



STRAPS, Mechanical Parts

Check

Hynix256MB :	R825_0	R824_1	R822_1	R820_1
Hynix128MB :	R825_0	R823_0	R822_1	R820_1
Hynix64MB :	R826_1	R823_0	R822_1	R820_1
Infineon256MB :	R825_0	R824_1	R822_1	R819_0
Infineon128MB :	R825_0	R823_0	R822_1	R819_0
Infineon64MB :	R826_1	R823_0	R822_1	R819_0

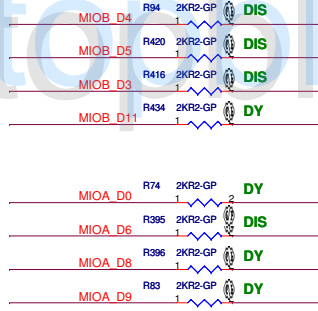


Bit Signal	Values
MIOA_D1: SUB_VENDOR	0 NO BIOS 1 READ FROM BIOS

For MEM strapping, Please use below table:

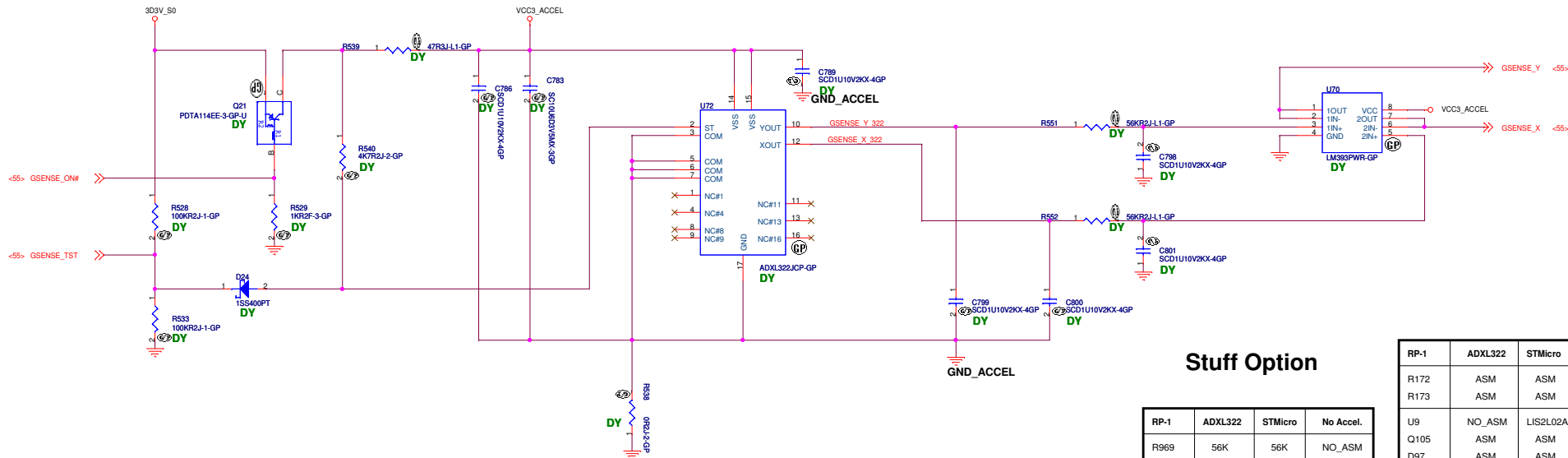
RAM_CFG[9.8.1.0]	Config	FB Bus Width	Definitions
0000			
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100			
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

<50> MIOA_D0	<< MIOA_D0
<50> MIOA_D1	<< MIOA_D1
<50> MIOA_D6	<< MIOA_D6
<50> MIOA_D8	<< MIOA_D8
<50> MIOA_D9	<< MIOA_D9
<50> MIOB_D0	<< MIOB_D0
<50> MIOB_D1	<< MIOB_D1
<50> MIOB_D3	<< MIOB_D3
<50> MIOB_D4	<< MIOB_D4
<50> MIOB_D5	<< MIOB_D5
<50> MIOB_D8	<< MIOB_D8
<50> MIOB_D9	<< MIOB_D9
<50> MIOB_D11	<< MIOB_D11



MIOB_D4: PCI_DEVID_0	
MIOB_D5: PCI_DEVID_1	1000 (default 0x00FC)
MIOB_D3: PCI_DEVID_2	
MIOB_D11: PCI_DEVID_3	0111 G72MV G72MZ=6, G73=8

MIOA_D0: PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED
MIOA_D6: 3GIO_PADCFG_LUT_ADDR[0]	
MIOA_D8: 3GIO_PADCFG_LUT_ADDR[1]	
MIOA_D9: 3GIO_PADCFG_LUT_ADDR[2]	001 DEFAULT



A-note 2.0 LED's Location and Sequence

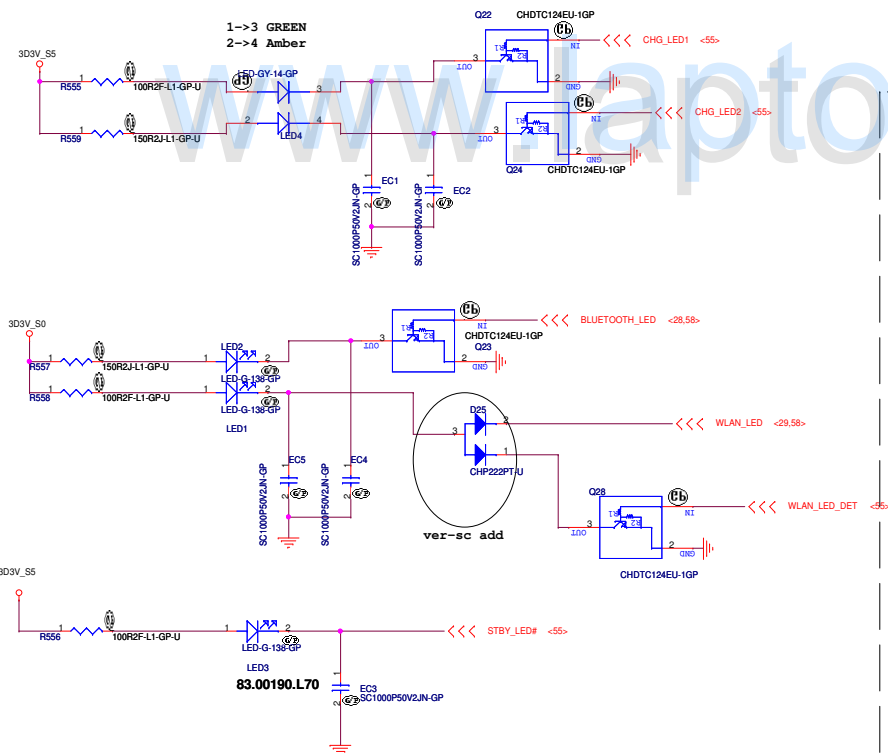
Left side Right side

WLAN Bluetooth Battery Suspend

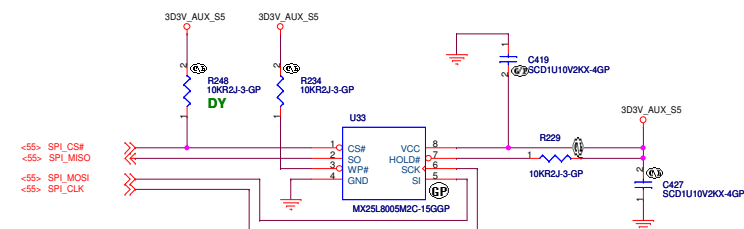
Stuff Option

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM



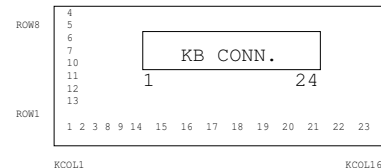
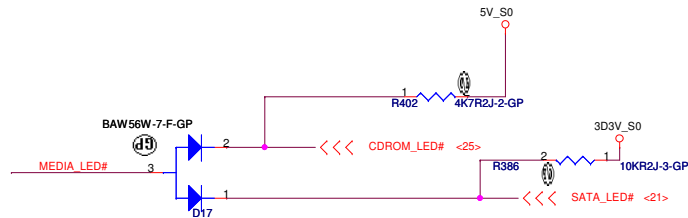
SPI ROM for System & KBC



1. MXIC MX25L8005M2C
2. WINBOND W25X80
3. SST 8Mbit72.25080.G01

A-NOTE2

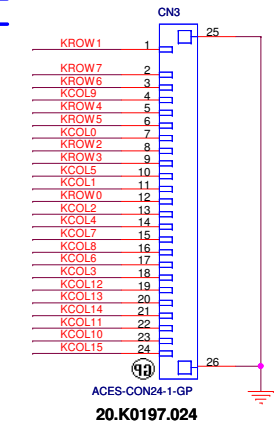
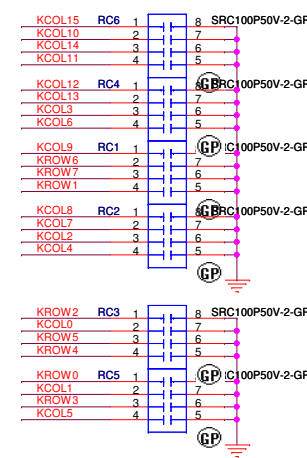
緯創資通 Wistron Corporation		
21F, 8B, Sec.1, Hei Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
G-sensor / SPI / LEDs		
File	Document Number	Rev
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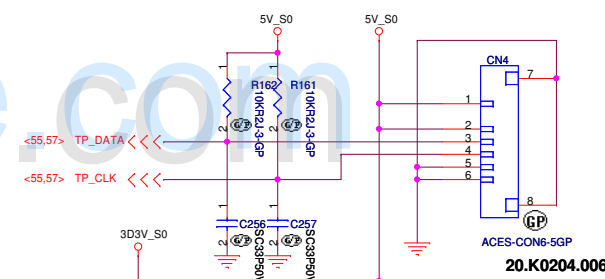
Internal Keyboard Connector

<55,57> KROW[0..7] <<<

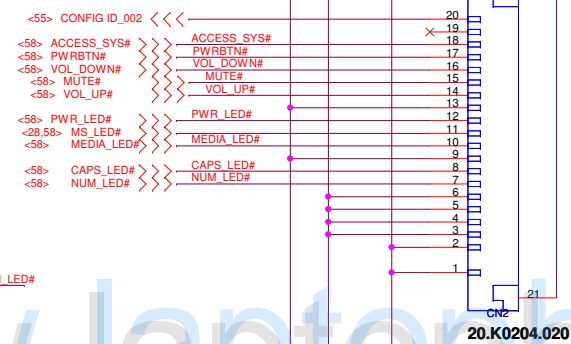
<55,57> KCOL[0..15] <<<



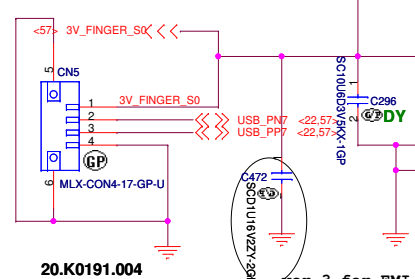
TouchPad Connector



Lanuch Board CNN



Finger Printer CNN

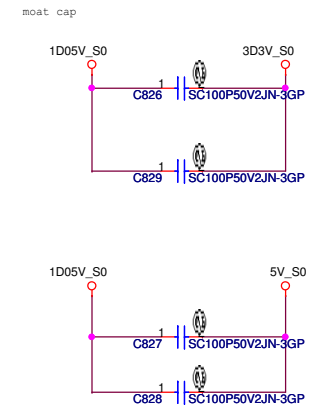
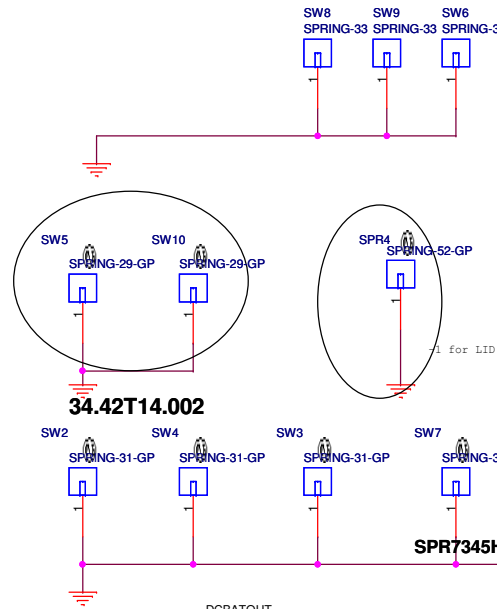
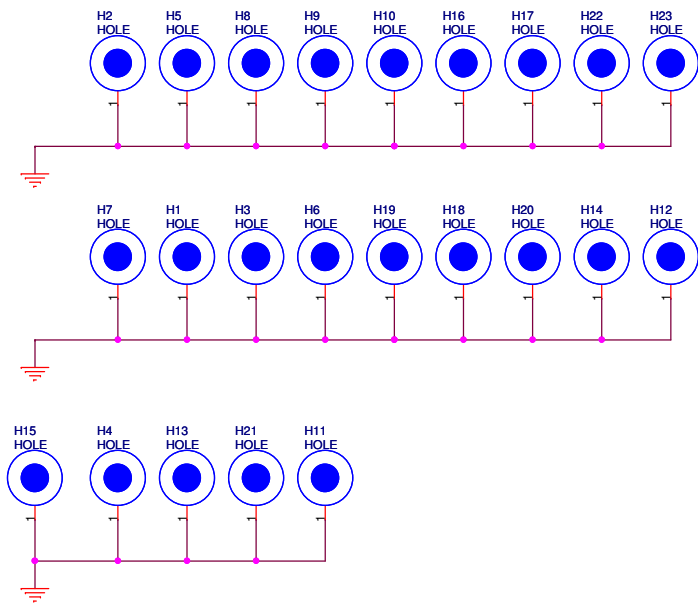


A-NOTE2

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Keyboard /Touch Pad			
Size A3	Document Number	Anote2.0 INTEL	
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34.42T14.002

For EMI solution

15pcs

EMI LAB2 add

ver-sc add

5pcs

8pcs

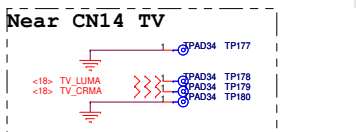
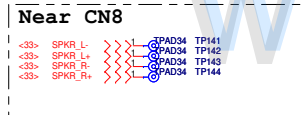
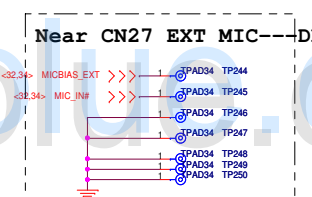
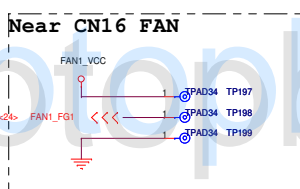
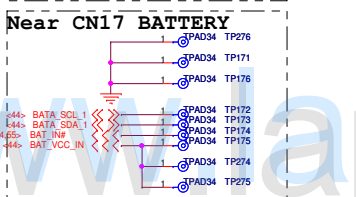
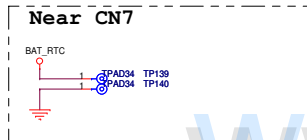
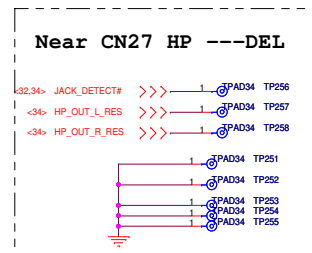
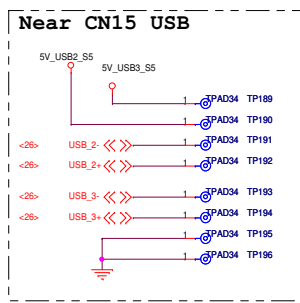
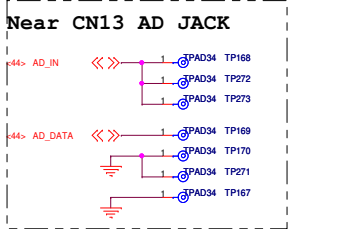
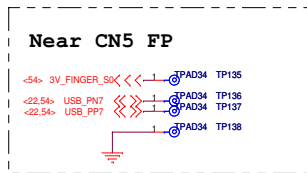
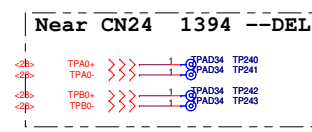
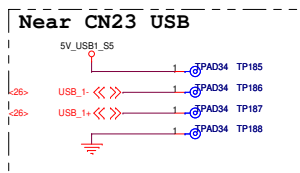
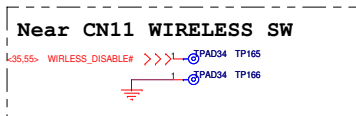
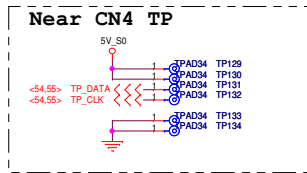
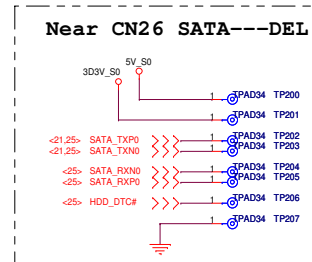
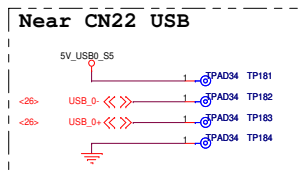
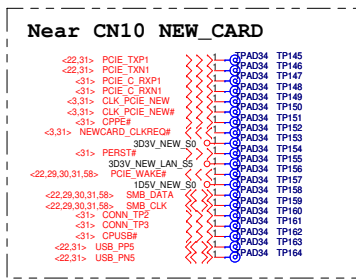
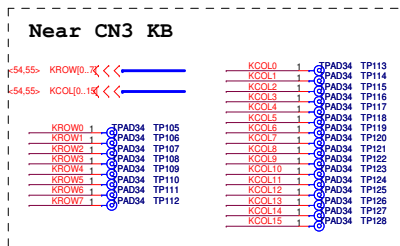
ver-sc add

A-NOTE2

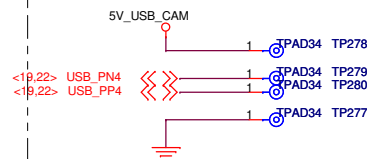
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Taipei Hsien 221, Taiwan, R.O.C.

Title			HOLE/ SPRING	
Size	Document Number	Anote2.0 INTEL		Rev
B				-1
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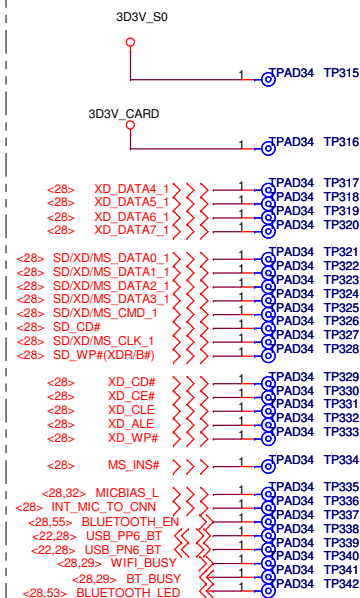
Near LCD CNN--CAM



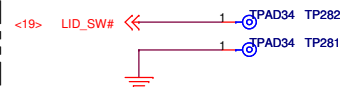
Modem



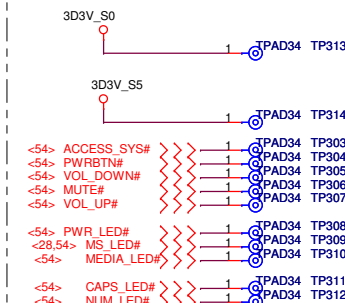
Daughter-BD



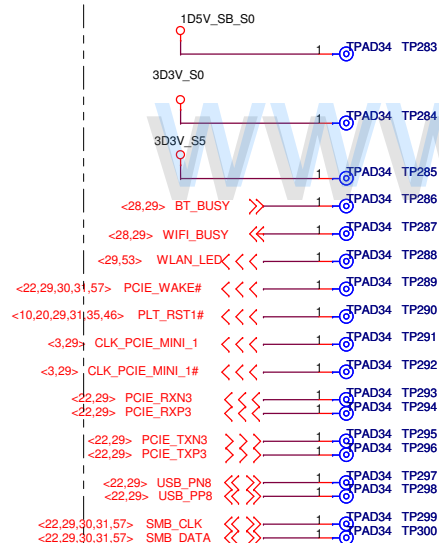
Near SW1



Launch-BD



Near CN25--Mini -PCIE



A-NOTE2

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
TEST_PAD		
Size B	Document Number	Rev
	Anote2.0 INTEL	-1
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